

nexus™

Asynchronous Interconnect
For Synchronous SoC Designs

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Agenda

- Motivation for Asynchronous Interconnect (1)
- Asynchronous Integrated Pipelining (1)
- Nexus Interconnect Architecture (4)
- Example Applications (4)
- Testing (4)
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- Conclusions (1)

Globally Asynchronous, Locally Synchronous

- **System-on-Chip designs usually integrate many cores with different clock domains.**
- **Asynchronous circuits can be used to interconnect multiple synchronous cores in a System-on-Chip design, eliminating global clock distribution and simplifying clock domain crossing.**
- **Fulcrum Microsystems' "Nexus" is a high speed on-chip interconnect:**
 - 16 port, 36 bit asynchronous crossbar
 - Asynchronous cross-chip channels
 - Async-sync clock domain converters
 - Runs at 1.35GHz in 130nm process

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Asynchronous Integrated Pipelining

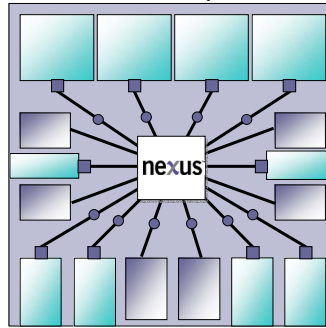
- **Developed at Caltech, licensed to Fulcrum.**
- **Delay-Insensitive timing model.**
 - Gates and wires can have arbitrary delays
- **4 phase 1of4 handshake.**
 - Uses 4 wires to send 2 bits
 - Plus an acknowledge wire for flow control
 - Returned to neutral between each data transfer
 - Self shielding
- **Precharge domino logic plus asynchronous handshaking circuitry.**
- **Low latency, high frequency, robust.**
- **Automatic power conservation, zero standby power.**

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Nexus System-on-Chip Interconnect

Generic Nexus Example



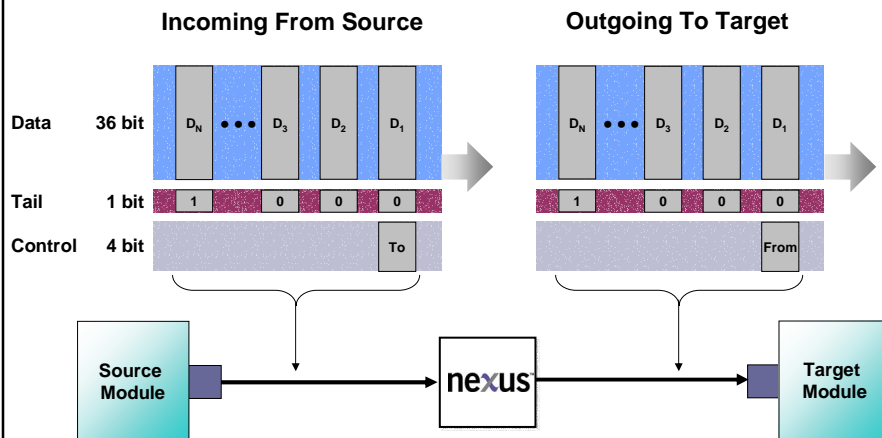
- Synchronous IP block
- Asynchronous IP block
- Pipelined repeater
- Clock domain converter

- Non-blocking crossbar
- 16 full-duplex ports
- Flow control extends through the crossbar
- Full speed arbitration
- Arbitrary-length “bursts”
- Bridges clock domains
- Scales in bit width and ports
- Process portable

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Nexus Burst Format



Arbitrary-length source-routed bursts provide flexibility

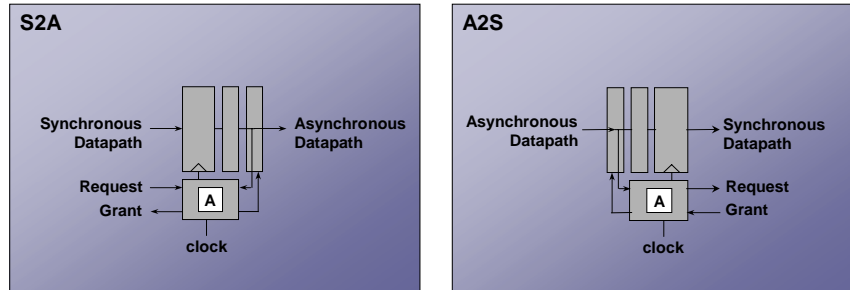
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Sync-to-Async Conversion

- **Synchronous Request / Grant FIFO protocol.**

- Data transferred if request and grant both high on rising edge of clock
- Compensates for any skew on asynchronous side
- Low latency: 1/2 to 3/2 clock cycles at A2S



Seamlessly Bridges Different Clock Domains

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Arbitration and Ordering

- **Unrelated sender/receiver links are completely independent.**
- **Bursts sent from multiple input ports to the same output port are serviced fairly by built-in arbitration circuitry.**
- **Bursts from A to B remain ordered.**
- **Producer-consumer and global-store-ordering satisfied.**
 - A sends X to B, A notifies C, C can read X from B
 - A writes X to B, A writes Y to C, if D reads Y from C, it can read X from B
- **Split transactions implement loads.**
 - Load request and load completion bursts
 - Load completions returned out-of-order

Can tunnel common bus and cache coherence protocols

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Example: Load/Store Systems

- **Option 1: Pure Master/Target Ports**

- Masters send Requests to Targets, which may return Completions
- Each port must either be a Master or a Target so that Completions are never blocked by Requests
- Devices which need to be both Masters and Targets are given two separate full-duplex ports
- Could use two separate Nexus crossbars

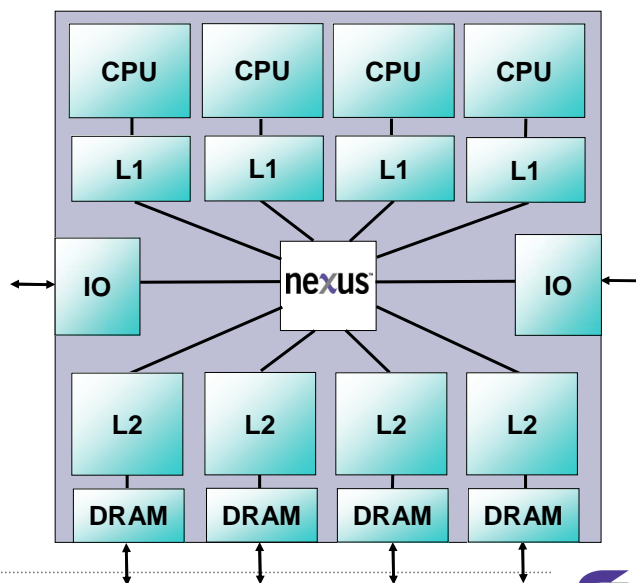
- **Option 2: Peers**

- Modules which are both Masters and Targets implement an internal buffer to hold Requests so that Completions can bypass them
- All Masters or Peers restrict number of outstanding Requests to avoid overflowing Request buffers

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Example: Multiprocessor SoC



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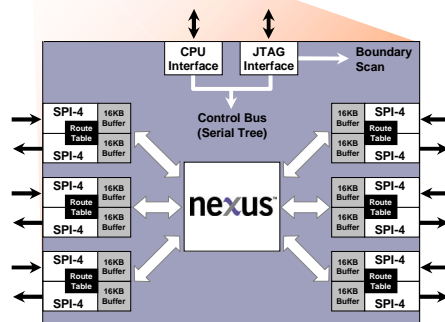
Example: Switch Fabric

- Each module maintains input/output queues for traffic to/from each other module.
- Data is sent from an input queue to an output queue over Nexus as a series of short bursts.
- Flow control credits for each output queue are sent backward.
- Eliminates head-of-line blocking.
- Segmentation, buffering, and overspeed optimize performance during congestion.
- Used in PivotPoint, Fulcrum's first chip product.

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PivotPoint Leverages Nexus



- **Flexible architecture**
 - 6 full-duplex SPI-4.2 interfaces
 - 16 channels per interface
 - Maps input interface/channel to output interface/channel
- **Optimized for performance**
 - Up to 14.4Gbps per interface
 - 32Gbps per Nexus port
 - 32KB full-speed buffers per port
 - Lossless flow control
- **Easily configurable**
 - 16-bit CPU interface
 - JTAG support
- **Modest size and power**
 - ~2 Watt per active interface
 - 1036 ball package

A true GALS SoC design

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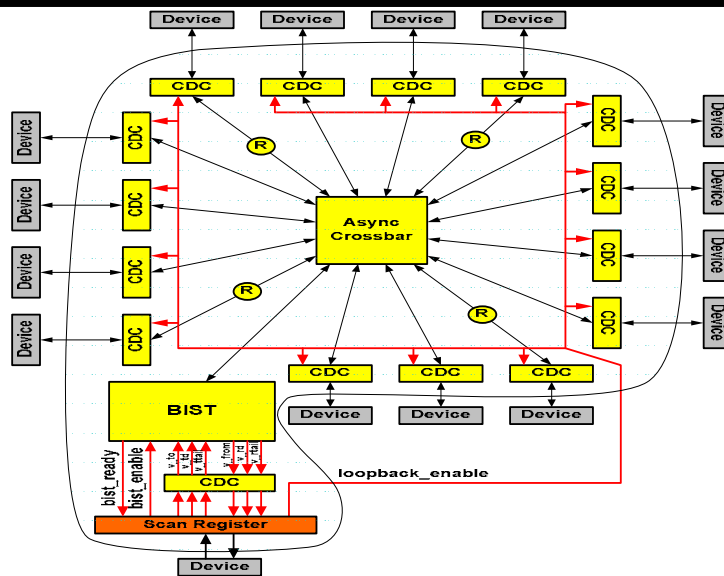


Fault and Delay Testing of Nexus

- Use a special Nexus port to assist testing.
- Can send a burst to port A, which reflects it to port B, which reflects it back to test port.
- Test port repeats each triangle several times.
- Final data is scanned after waiting a suitable time.
- Supports fault testing, delay testing, and speed binning with minimal additional circuitry.

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Testing Diagram



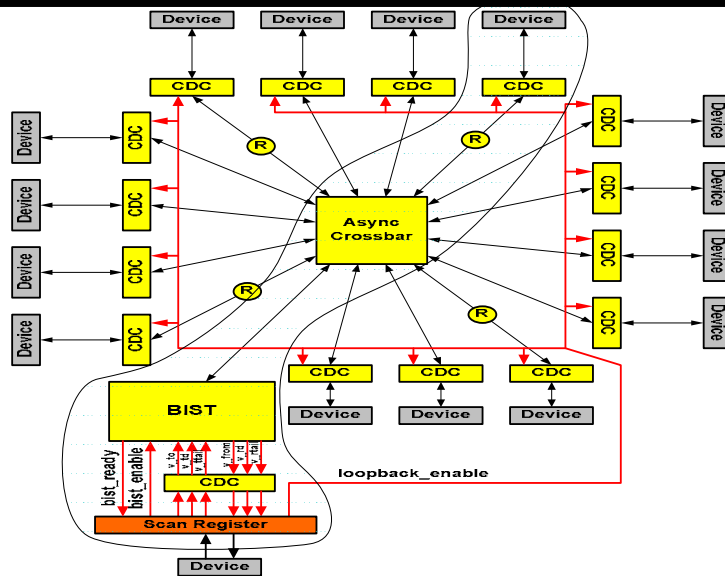
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Testing the Synchronous Modules

- Use standard synchronous scan chain for internal fault testing.
- For at-speed testing of each module, can redirect all traffic from that module to the test port.
- The test port can be connected to an external tester (with reduced pin-count and reduced speed).
- Lock the module's clock to a multiple of the test clock.
- Each module is independently tested at its maximum frequency.
- All behavior deterministic during testing.

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Testing Diagram

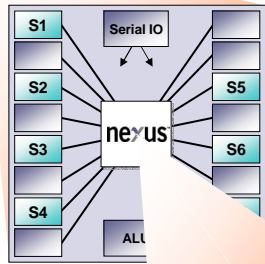


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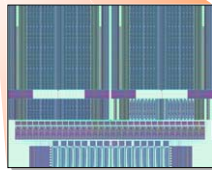
Nexus Silicon Validation



Block diagram of Nexus Validation Chip



Plot of Nexus crossbar



TSMC 130nm LV Results

Process	V	GHz	ns	pJ/bit
Low-K	1.2	1.35	2.0	10.4
Low-K	1.0	1.11	2.4	7.0
FSG	1.2	1.10	2.5	11.2
FSG	1.0	0.87	3.1	7.6

Crossbar area: 1.75mm²

Total interconnect area: 4.15mm²

Peak cross-section bandwidth: 778Gb/s

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Conclusion

- Nexus is an asynchronous crossbar interconnect designed to connect up to 16 synchronous modules in a SoC.
- Nexus can be used to implement load/store systems as well as switch fabrics.
- Systems using Nexus can be tested with standard equipment.
- Nexus runs up to 1.35GHz in TSMC 130nm.
- Asynchronous interconnect is now a viable solution for very high performance SoC designs.

Asynchronous design has finally arrived!

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Thank You!

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