

High-speed, high-bandwidth DRAM memory bus with Crosstalk Transfer Logic (XTL) interface

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1

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Outline

- Requirements of server memory system
- Background of high-speed interconnect
- Mechanism of XTL
- Design of evaluation system
 - 0.15- μ m process TEST chip (hysteresis receiver)
 - 8 modules mountable PCB w/ folding coupler
- XTL Experimental result
- Conclusion

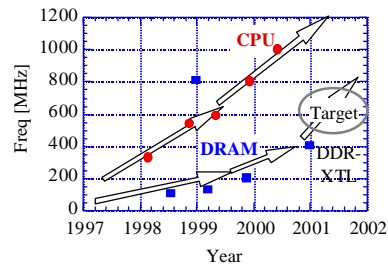
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Requirements of server memory system

- Memory system for high-performance workstation and server
 - High band width
 - Large capacity
 - Low latency access
 - Low power
 - High availability
 - Cost



3

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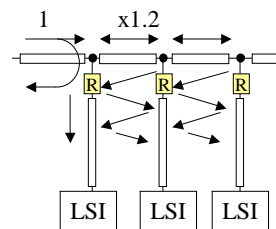
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Background of high-speed interconnect

- Bus cheaper than point-to-point
 - Low pin count and small real estate owing to sharing signal
- However, hard to manage trade-off speed-up and noise
- ISI (Inter Symbol Interference) limits speed-up
 - Multi- reflections between branch points
 - Important impedance flatness
- Information in a transition of datum
 - Rising: L→ H, Falling: H→ L
 - No change: Stable datum (L→ L/H→ H)



information information



Multi-reflection noise on bus

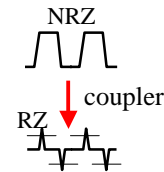
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Features of XTL

- Many modules mountable a bus: 4 to 8 DIMM (conventionally 2 ~ 4)
- High speed operation: > 500Mbps
- Very small reflection noise (lesser ISI)
 - Signal transmitter: Directional coupler formed in PCB
 - Small impedance violation
- Transition data capture (NRZ → RZ)
- Hot Swappable
 - DC Isolation (signal)
- C-MOS technology
 - Push-pull driver (same as conventional SSTL driver)
 - Hysteresis receiver
- Low cost PCB (2 signal layers)



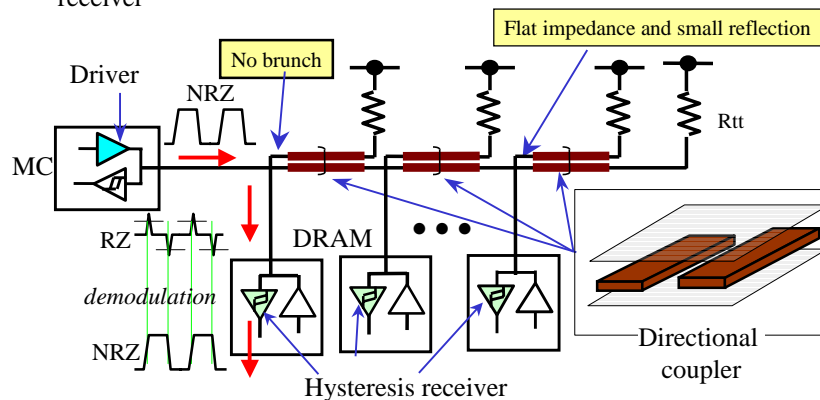
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Mechanism of XTL (WRITE mode)

- No branch on a mainline: Impedance flat of the mainline
- Drive NRZ signal from Memory Controller
- Transform to RZ signal at coupler and Demodulate by hysteresis receiver



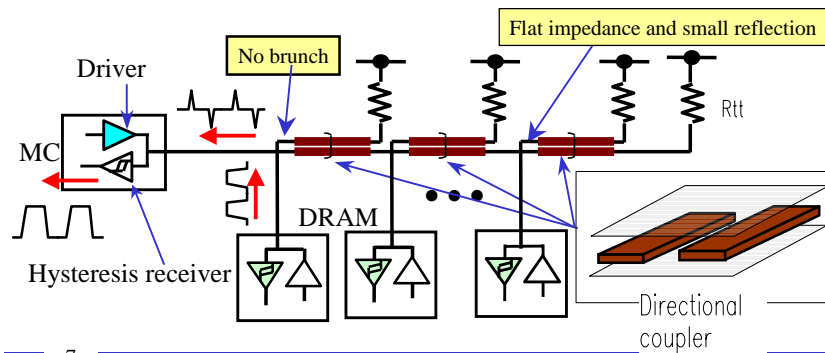
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Mechanism of XTL (READ mode)

- READ mode
 - Opposite direction, but the same mechanism as WRITE mode
 - DC isolation



7

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Design of XTL evaluation system

Evaluate XTL performance for DRAM memory bus

- 0.15- μm DRAM process chip (HS-TEG)
- I/O circuits
 - Driver: Impedance and slew-rate controllable
 - Receiver: Controllable hysteresis
 - Vernier timing controller
- PCB (Motherboard and DIMM)
 - 8 modules mountable motherboard
 - 2 layers for folding coupler (total 8 layers stacking)
 - Low cost using conventional technology
 - Line width and spacing = 100 / 100 μm [4 mil]

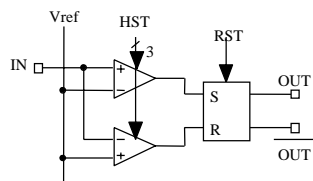
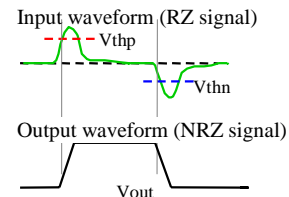
8

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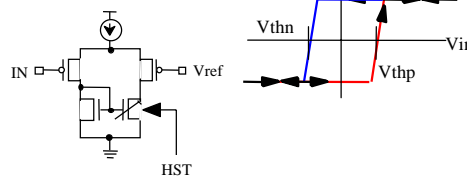
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Receiver design

- Demodulate from RZ signal to NRZ
- High-speed operational receiver
 - Receiver consists 2 controllable-offset comparators + RS-FF
 - Hysteresis offset: $\pm 50, \pm 100, \pm 150$ mV



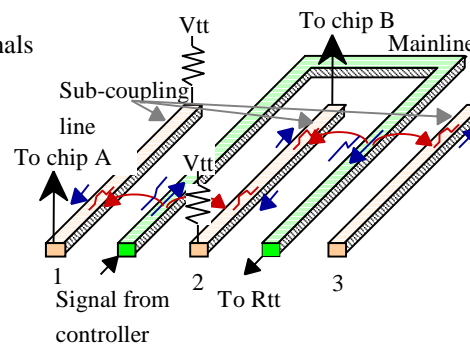
(a) Hysteresis receiver circuit



(b) Controllable offset comparator

Folding Coupler

- Low cost low noise folding line structure
 - Reduce layers
 - High density
 - Avoid noise from adjacent signals
- Parameters
 - Coupler 40 mm [1.57"] length
 - Z_0 (mainline) = 75Ω
 - Coupling coeff. $\sim 25\%$
 - L/S = 100/100 μm [4mil]



XTL coupler layout on a PCB layer

HS-TEG test chip

Features:

- XTL interface test chip: 0.15- μ m process
- 54-ball CSP (Chips Scale Package)
- No DRAM cell



DIE photo of HS-TEG chip

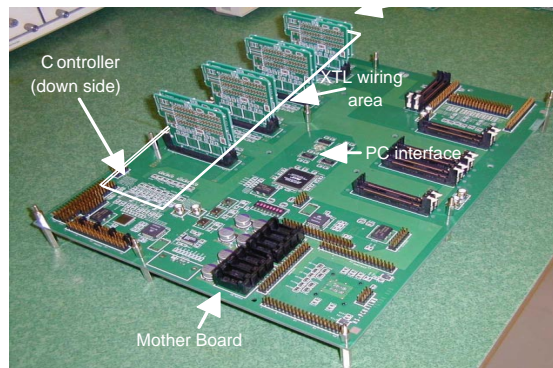
11

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Evaluation PCB

- 8 modules mountable
- 4 bytes bus width
- Low cost PCB using conventional technology
 - L/S = 100/100 μ m [4 mil]
 - 2 Signal layers (total 8 layers)



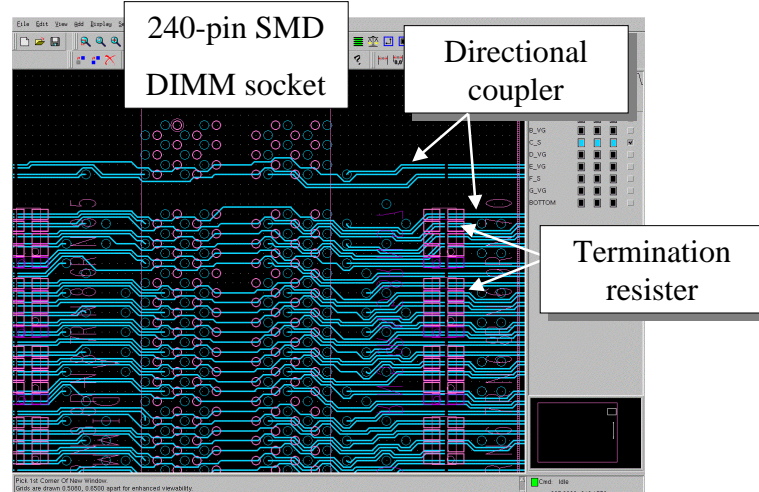
Test board; a mother board and mounted 8 modules; All modules mounted 4 HS-TEG chips.

12

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Layout of XTL signals



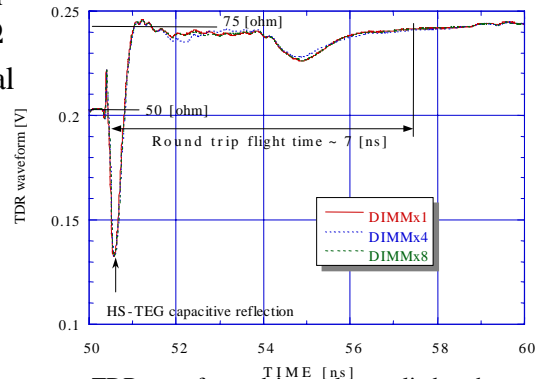
13

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Experimental results (1)

- Impedance measured when 1,4 and 8 DIMMs loaded
- Impedance variation of mainline $< \pm 6 \Omega$
→ ISI effect minimal



TDR : Time Domain Reflectometry)

TDR waveform: drive pulse applied to the ball of the HS-TEG of the mainline

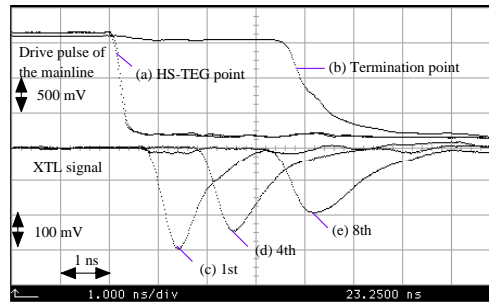
14

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Experimental results (2)

- XTL Signaling
 - Drive falling time : 181 - 947 ps [20-80%]
 - XTL signal: 305 - 197 mV (@ 8th module)
 - Coupling ration: $K_b \sim 24\%$ (= XTL signal / Drive pulse)



Drive pulse and XTL signal

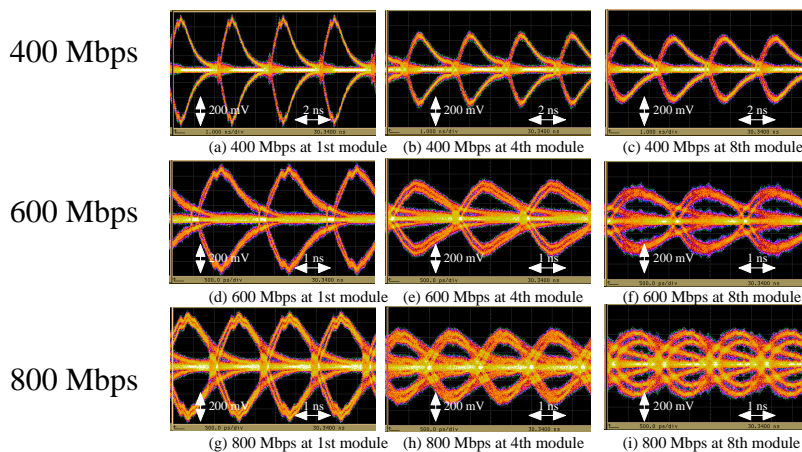
15

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Experimental results (3)

- Eye diagram of XTL signaling (write mode)



16

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Experimental results (4)

- Max. operation frequency w/ Error Rate Tester
 - Adjacent signals drove
 - First module: over 600 Mbps
 - 8th modules: over 500 Mbps
 - Adjacent noise: 49.6 mV [600 Mbps / 4th module]

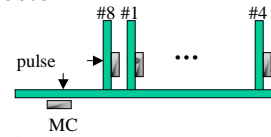


Table 1 Maximum operation frequency

	Write	Read
DIMM#1 (Near End)	612 Mbps	604 Mbps
DIMM#8 (Far end)	523 Mbps	524 Mbps

Typ. Condition
Room Temp.
BERT < 10⁻¹²

Conclusion

- XTL interconnection applied to DRAM memory bus
- Evaluation results
 - Over 500 Mbps operation with 8 modules both read and write
 - Test chip
 - 0.15- μ m DRAM process
 - Receiver: Controllable offset $\pm 50, \pm 100, \pm 150$ mV
 - Test board
 - Only two signal layers for four byte bus
 - Folding coupler reduces signal layers and avoid adjacent noise
- Hot swappable (DC isolated signal)

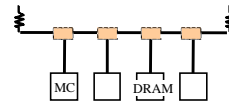
Appendix

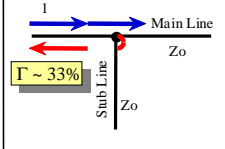
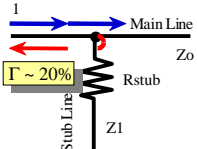
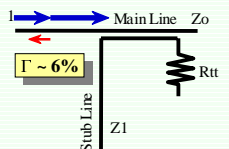
- Signaling of various memory buses
- Preamble of DQ/DQS
- Clock routing of DQ / DQS

Signaling of various memory buses

- DDR-SDRAM interface comparison

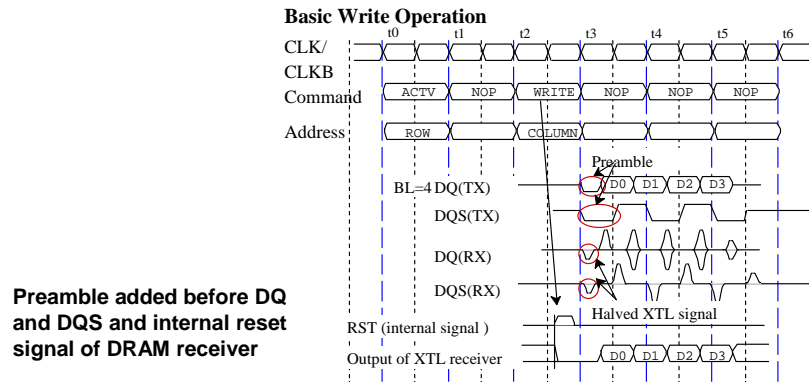
– Multi-reflection causes Inter-symbol interference degradation



Interface	LVTTL(PC100/133) Low Voltage TTL	SSTL(DDR-II) Stub Series Terminated Logic	XTL (proposal) Crosstalk Transceiver Logic
Driver	push-pull/open-drain	push-pull	push-pull
Receiver	Single-end/Differential	Differential	Hysteresis
Branch	Direct branch	Series Termination	Directional coupler
Reflection	Large ~ 33 %	Medium ~ 20 %	Small ~ 6 %
Bus Branch			

Preamble of DQ/DQS

- Low-state preamble before DQ/DQS
 - Halved XTL signal from idle state to first data



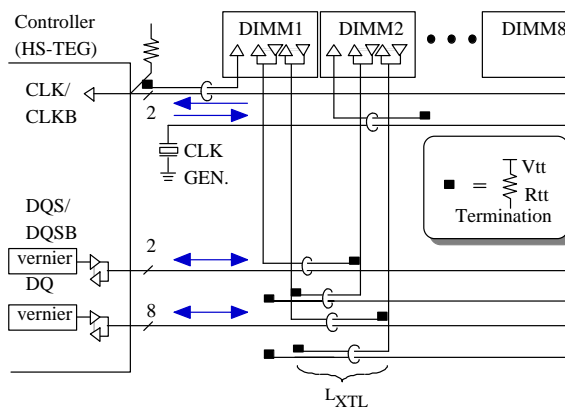
21

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Clock routing of DQ / DQS

- Read DQ/DQS same as CLK



22

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