High-speed, high-bandwidth DRAM memory bus with Crosstalk Transfer Logic (XTL) interface

Outline

• Requirements of server memory system
• Background of high-speed interconnect
• Mechanism of XTL
• Design of evaluation system
  – 0.15-µm process TEST chip (hysteresis receiver)
  – 8 modules mountable PCB w/ folding coupler
• XTL Experimental result
• Conclusion
Requirements of server memory system

- Memory system for high-performance workstation and server
  - High band width
  - Large capacity
  - Low latency access
  - Low power
  - High availability
  - Cost

Background of high-speed interconnect

- Bus cheaper than point-to-point
  - Low pin count and small real estate owing to sharing signal
- However, hard to manage trade-off speed-up and noise
- ISI (Inter Symbol Interference) limits speed-up
  - Multi- reflections between branch points
  - Important impedance flatness
- Information in a transition of datum
  - Rising: L→H, Falling: H→L
  - No change: Stable datum (L→L/H→H)

Multi-reflection noise on bus
Features of XTL

- Many modules mountable a bus: 4 to 8 DIMM (conventionally 2 ~ 4)
- High speed operation: > 500Mbps
- Very small reflection noise (lesser ISI)
  - Signal transmitter: Directional coupler formed in PCB
  - Small impedance violation
- Transition data capture (NRZ → RZ)
- Hot Swappable
  - DC Isolation (signal)
- C-MOS technology
  - Push-pull driver (same as conventional SSTL driver)
  - Hysteresis receiver
- Low cost PCB (2 signal layers)

Mechanism of XTL (WRITE mode)

- No branch on a mainline: Impedance flat of the mainline
- Drive NRZ signal from Memory Controller
- Transform to RZ signal at coupler and Demodulate by hysteresis receiver
Mechanism of XTL (READ mode)

- **READ mode**
  - Opposite direction, but the same mechanism as WRITE mode
  - DC isolation

Design of XTL evaluation system

Evaluate XTL performance for DRAM memory bus

- 0.15-\(\mu\)m DRAM process chip (HS-TEG)
- I/O circuits
  - Driver: Impedance and slew-rate controllable
  - Receiver: Controllable hysteresis
  - Vernier timing controller
- PCB (Motherboard and DIMM)
  - 8 modules mountable motherboard
  - 2 layers for folding coupler (total 8 layers stacking)
  - Low cost using conventional technology
    - Line width and spacing = 100 / 100 \(\mu\) m [4 mil]
Receiver design

- Demodulate from RZ signal to NRZ
- High-speed operational receiver
  - Receiver consists 2 controllable-offset comparators + RS-FF
  - Hysteresis offset: ± 50, ± 100, ± 150 mV

(a) Hysteresis receiver circuit
(b) Controllable offset comparator

Folding Coupler

- Low cost low noise folding line structure
  - Reduce layers
  - High density
  - Avoid noise from adjacent signals
- Parameters
  - Coupler 40 mm [1.57’] length
  - Zo (mainline) = 75 Ω
  - Coupling coeff. ~ 25 %
  - L/S = 100/100 µm [4mil]

XTL coupler layout on a PCB layer
HS-TEG test chip

Features:
- XTL interface test chip: 0.15-μm process
- 54-ball CSP (Chips Scale Package)
- No DRAM cell

Evaluation PCB

- 8 modules mountable
- 4 bytes bus width
- Low cost PCB using conventional technology
  - L/S = 100/100 μm [4 mil]
  - 2 Signal layers (total 8 layers)
Layout of XTL signals

- 240-pin SMD DIMM socket
- Directional coupler
- Termination resistor

Experimental results (1)

- Impedance measured when 1, 4 and 8 DIMMs loaded
- Impedance variation of mainline $< \pm 6 \, \Omega$
  $\rightarrow$ ISI effect minimal

TDR waveform: drive pulse applied to the ball of the HS-TEG of the mainline

TDR : Time Domain Reflectometry

- Round trip flight time ~ 7 [ns]

<table>
<thead>
<tr>
<th>DIMM</th>
<th>50 [\Omega]</th>
<th>75 [\Omega]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIMMx1</td>
<td>50 [\Omega]</td>
<td>75 [\Omega]</td>
</tr>
<tr>
<td>DIMMx4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DIMMx8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Experimental results (2)

- **XTL Signaling**
  - Drive falling time: 181 - 947 ps [20-80%]
  - XTL signal: 305 - 197 mV (@ 8th module)
  - Coupling ration: \(K_b \approx 24\%\) (= XTL signal / Drive pulse)

![Drive pulse and XTL signal](image)

Experimental results (3)

- **Eye diagram of XTL signaling (write mode)**

400 Mbps
- (a) 400 Mbps at 1st module
- (b) 400 Mbps at 4th module
- (c) 400 Mbps at 8th module

600 Mbps
- (d) 600 Mbps at 1st module
- (e) 600 Mbps at 4th module
- (f) 600 Mbps at 8th module

800 Mbps
- (g) 800 Mbps at 1st module
- (h) 800 Mbps at 4th module
- (i) 800 Mbps at 8th module
Experimental results (4)

- Max. operation frequency w/ Error Rate Tester
  - Adjacent signals drove
  - First module: over 600 Mbps
  - 8th modules: over 500 Mbps
  - Adjacent noise: 49.6 mV [600 Mbps / 4th module]

<table>
<thead>
<tr>
<th></th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIMM#1 (Near End)</td>
<td>612 Mbps</td>
<td>604 Mbps</td>
</tr>
<tr>
<td>DIMM#8 (Far end)</td>
<td>523 Mbps</td>
<td>524 Mbps</td>
</tr>
</tbody>
</table>

Typ. Condition
Room Temp. BERT < 10^{-12}

Conclusion

- XTL interconnection applied to DRAM memory bus
- Evaluation results
  - Over 500 Mbps operation with 8 modules both read and write
  - Test chip
    - 0.15-µm DRAM process
    - Receiver: Controllable offset ± 50, ± 100, ± 150 mV
  - Test board
    - Only two signal layers for four byte bus
    - Folding coupler reduces signal layers and avoid adjacent noise
- Hot swappable (DC isolated signal)
Appendix

- Signaling of various memory buses
- Preamble of DQ/DQS
- Clock routing of DQ / DQS

## Signaling of various memory buses

### DDR-SDRAM interface comparison

- Multi-reflection causes Inter-symbol interference degradation

<table>
<thead>
<tr>
<th>Interface</th>
<th>LVSTL(PC100/133)</th>
<th>SSTL(DDR-II)</th>
<th>XTL (proposal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Driver</td>
<td>push-pull/open-drain</td>
<td>push-pull</td>
<td>push-pull</td>
</tr>
<tr>
<td>Receiver</td>
<td>Single-end/Differential</td>
<td>Differential</td>
<td>Hysteresis</td>
</tr>
<tr>
<td>Branch</td>
<td>Direct branch</td>
<td>Series Termination</td>
<td>Directional coupler</td>
</tr>
<tr>
<td>Reflection</td>
<td>Large ~ 33 %</td>
<td>Medium ~ 20 %</td>
<td>Small ~ 6 %</td>
</tr>
<tr>
<td>Bus Branch</td>
<td>Γ ~ 33%</td>
<td>Γ ~ 20%</td>
<td>Γ ~ 6%</td>
</tr>
</tbody>
</table>

### Diagram

![Diagram of signaling](image-url)
Preamble of DQ/DQS

- Low-state preamble before DQ/DQS
  - Halved XTL signal from idle state to first data

Clock routing of DQ/DQS

- Read DQ/DQS same as CLK