

Optical Interconnection as an IP Macro of COMS LSIs (OIP)

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1. Introduction

Optical interconnection as an IP* macro of CMOS LSIs (OIP)

*IP: Intellectual Property

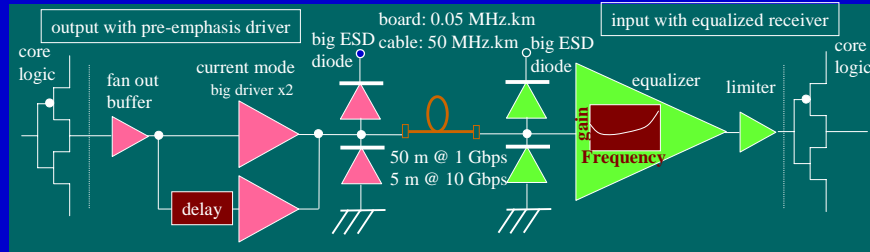
- Background
- Objective
- What is an OIP?
- Who benefits?

Background

system LSI needs 1-10 Gbps high-speed interface.

typical high-speed electrical interface

CML, LVDS

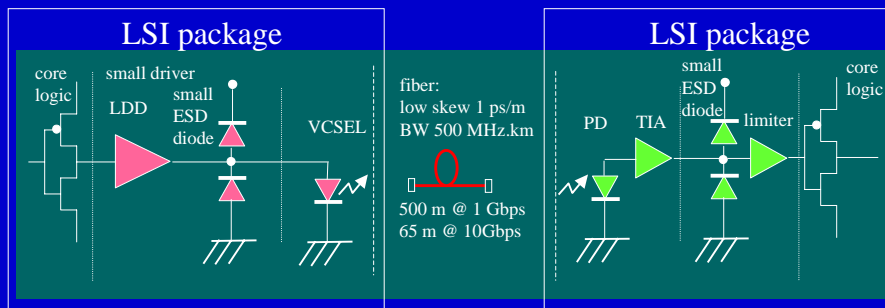


I/Os consume higher power because current mode and high drivable.
 Pre-emphasis and/or equalizer consume excessive power.
 Big ESD protection diodes prevent high-speed operation.
 Designing PWB is difficult, cable length is limited, determined.

Objective

Tera-bit throughput switch LSI

low-power and high-speed interface by in-package optics

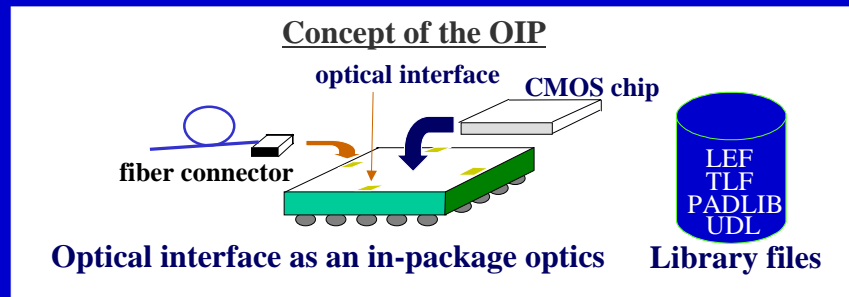


PWB, cabling become easier because all high-speed signals are optical.
 Optical interface is included in the conventional design of CMOS-LSI.

What is an OIP?

OIP : Optical interconnection as an IP macro of CMOS LSI

IP (Intellectual Property) : reused functional circuit block



Preparing optical interface as an in-package optics.
Integrating it in a conventional CMOS design

Who benefits ?

system designer

use high-speed optics
compact system

opt-module

new inter LSI market

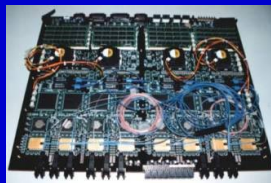
CMOS vender

realize higher-speed I/O

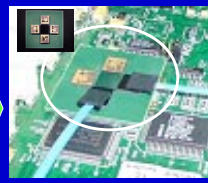
I/O 64 Gb/s

4 pair of
Array TX, RX,
(8 x 1 Gbps)
+ 8 SER/DES

T. Yoshikawa et.al.
Photon. Tech. Lett.
Vol. 9, 1627, '97.



430 x 540 mm



35 x 35 mm

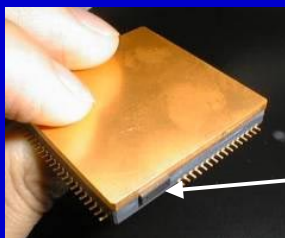
I/O 100 Gb/s

3.125 Gbps
16 x 16 SW
with opt-
interface

2. Concept Model

- MCM package
- 1000BASE-SX Network Interface Card

MCM type OIP Package



40 x 40 x 6 mm (same as 304-pin QFP)

88 electrical pin

Optical Connector (12 MT)

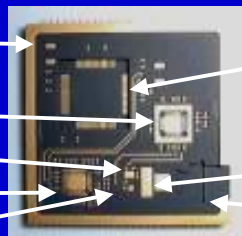
ceramic package

limiter amp

MSM-OEIC

LDD

VCSEL



land for PQFP
(SER/DES)

P-WG

MT receptacle

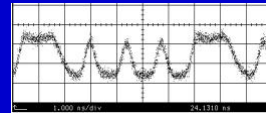
Implemented 1000BASE-SX

graphic card OIP-LSI NIC

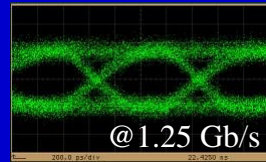


64 x 66 PCI

mother board



TX optical output



MSM-OEIC output (RX)

The ceramic package was expensive and assembly yield was low.

The optical interface should be assembled on other small substrate.

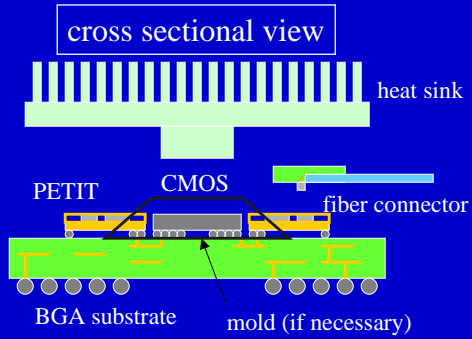
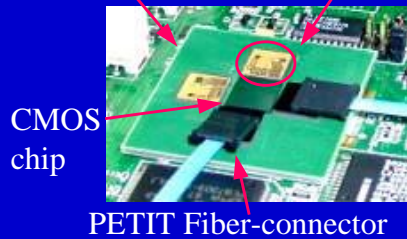
3. PETIT

Photonic and Electronic Tied InTerface

- BGA package with PETIT
- PETIT configuration
- link budget
- LDD in CMOS
- TIA
- Sub assembly, optics
- PETIT connector
- BGA substrate

BGA type OIP Package

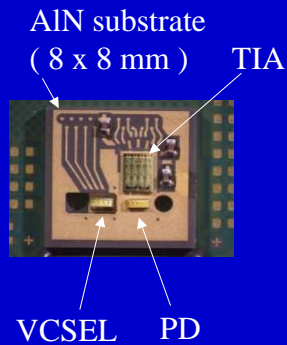
BGA substrate
(35 x 35 mm standard 352-pin) PETIT
(8 x 8 mm)



All optical and analog chips are assembled on the ceramic substrate.
In-package optics ← Mounting PETIT directly on a BGA substrate.

PETITI Configuration

12.5 Gbps full-duplex in 8 x 8 mm size

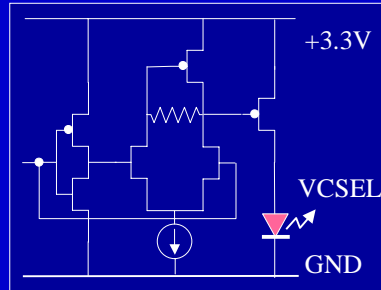


12.5 Gb/s full duplex
8 x 8 mm ceramic (AlN)
P (typ) 1.2 W (V_{dd} 3.3 V)

TX : 4 x 3.125 Gbps
850-nm VCSEL
no LDD (included in CMOS)
RX: 4 x 3.125 Gbps
MSM-PD (GaAs)
TIA (GaAs)

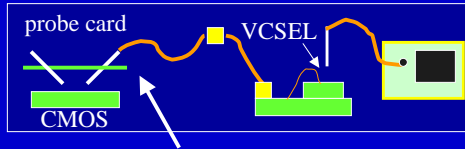
TX (LDD in CMOS and VCSEL)

CMOS: NEC's UR2H (0.25 μm)

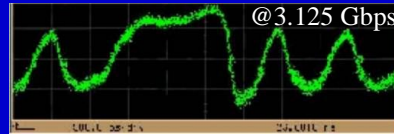


0.25 μm CMOS

similar circuit with OETC
(cf. T. C. Banwell, et. al. J. Quant. Electron. 29., 635, '93)



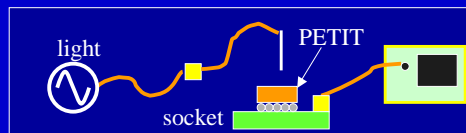
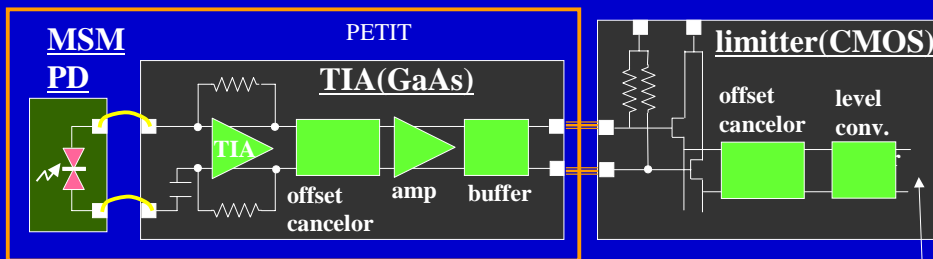
(probe card: noisy, BW ~ 1.0 GHz)



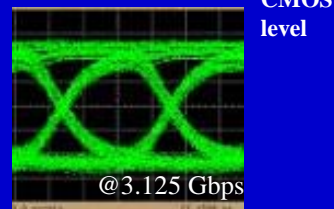
8b10b-coded and muxed D0.0

RX (TIA (GaAs) and PD)

GaAs: NEC's GES01(0.2 μm) CMOS: UR2H (0.25 μm)



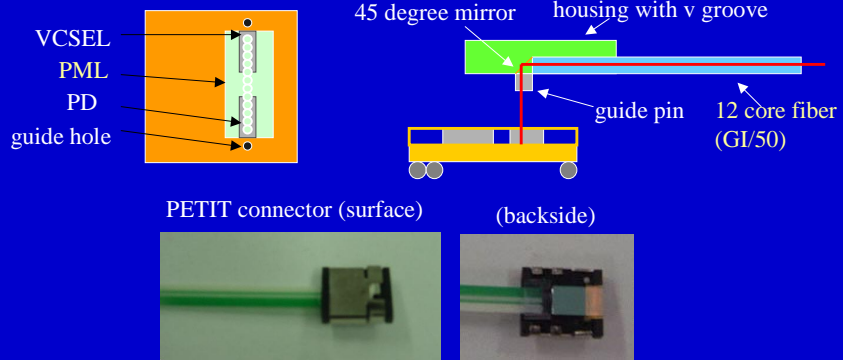
BW of the socket is ~ 1.5 GHz



RX output of PETIT

Optics

PETIT and PETIT connector



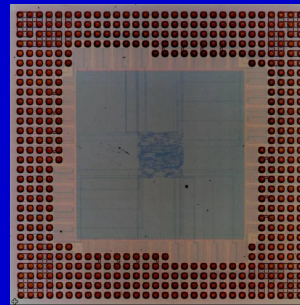
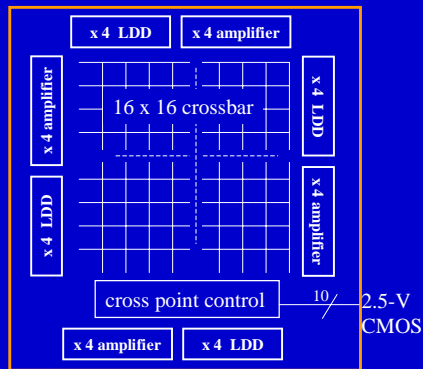
Commercial MT connector can be used.

4. CMOS

- Cross-point switch
- Multi channel SERDES

Cross Point Switch

3.125 Gb/s 16 x 16 NEC UR2H (0.25 μ m)



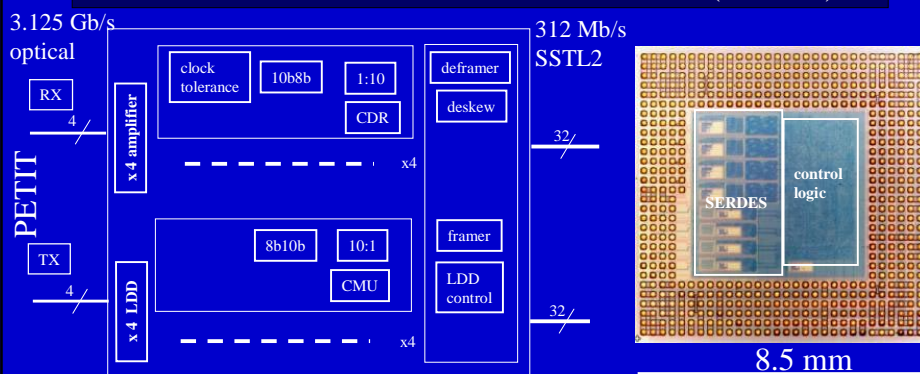
8.5 mm

250- μ m pitch solder bump

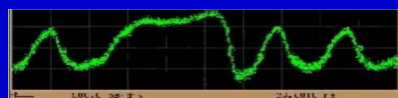
All high-speed signals are optically Input and output via PETIT

Multi Channel SERDES

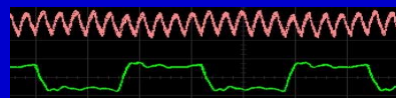
4 x 3.125 Gb/s SERDES NEC UR2H (0.25 μ m)



8.5 mm



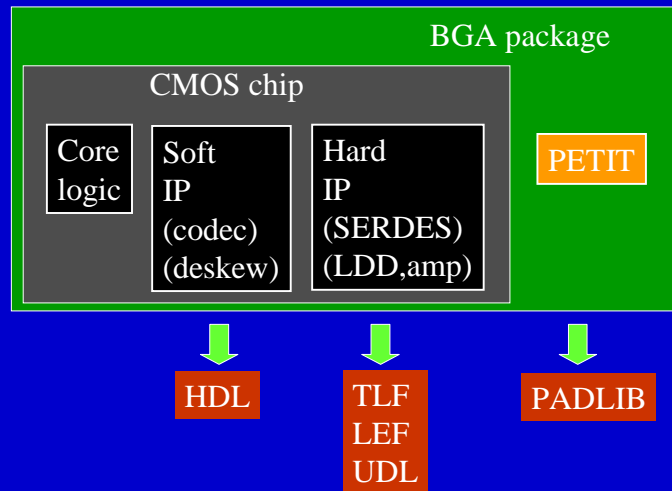
coded and multiplexed D0.0 (opt)



de-multiplexed and decoded 1,1,0,0

5. Library files

conventional cell-based ASIC design flow

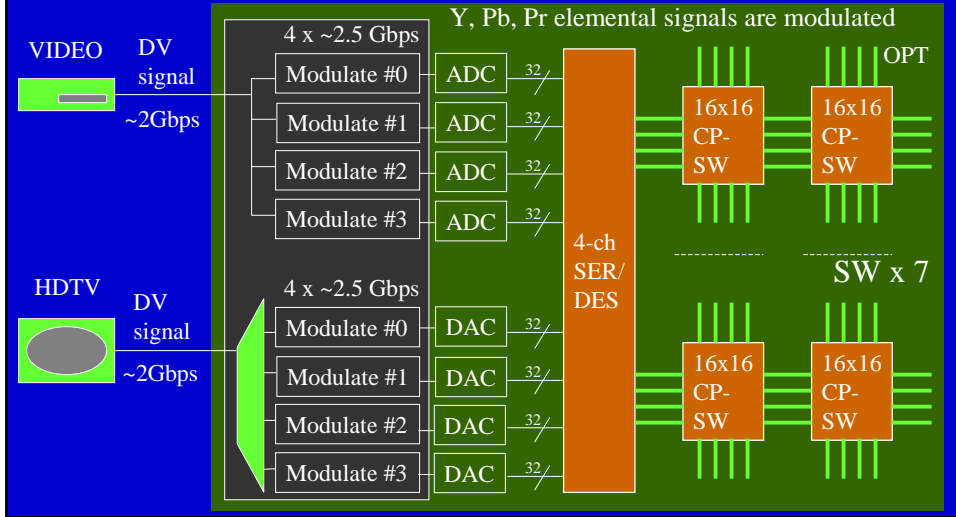


6. HDTV Switcher

- Block diagram
- PWB, lack

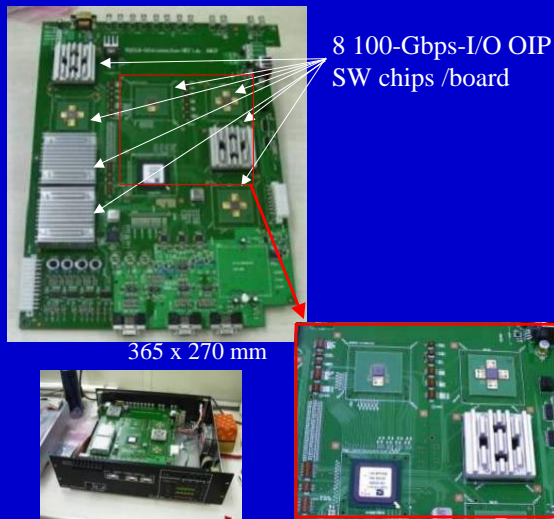
Block Diagram

Demonstrating 10-Gb/s interconnection and compact implementation.



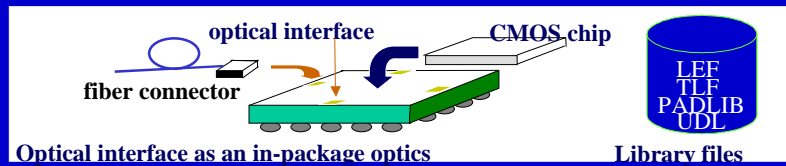
PWB, Lack

800-Gbps-I/O / board



7. Summary

(1) We developed OIP

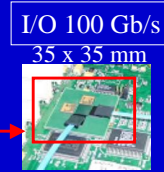
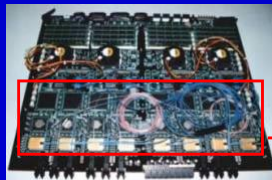


(2) PETIT realized 12.5 Gb/s duplex optical interface in 8 x 8 mm.

(3) 100 Gb/s optical I/O chip was developed by using OIP.

I/O 64 Gb/s 430 x 540 mm

I/O 800 Gb/s 365 x 270 mm



Acknowledgements

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