1. Introduction

Optical interconnection as an IP* macro of CMOS LSIs (OIP)

*IP: Intellectual Property

- Background
- Objective
- What is an OIP?
- Who benefits?
system LSI needs 1-10 Gbps high-speed interface.

I/Os consume higher power because current mode and high drivable. Pre-emphasis and/or equalizer consume excessive power. Big ESD protection diodes prevent high-speed operation. Designing PWB is difficult, cable length is limited, determined.

objective
Tera-bit throughput switch LSI

low-power and high-speed interface by in-package optics

PWB, cabling become easier because all high-speed signals are optical. Optical interface is included in the conventional design of CMOS-LSI.
What is an OIP?

OIP: Optical interconnection as an IP macro of CMOS LSI
IP (Intellectual Property): reused functional circuit block

Concept of the OIP
- Optical interface
- CMOS chip
- Fiber connector

Preparing optical interface as an in-package optics.
Integrating it in a conventional CMOS design

Who benefits?

- **System Designer**
  - Use high-speed optics
  - Compact system

- **Opt-Module**
  - New inter LSI market

- **CMOS Vendor**
  - Realize higher-speed I/O

I/O 64 Gb/s
- 4 pair of Array TX, RX
  - (8 x 1 Gbps)
  - + 8 SER/DES

I/O 100 Gb/s
- 3.125 Gbps
- 16 x16 SW with opt-interface

I/O 64 Gb/s
- 430 x 540 mm
- 35 x 35 mm

I/O 100 Gb/s
- 430 x 540 mm
- 35 x 35 mm
2. Concept Model

- MCM package
- 1000BASE-SX Network Interface Card

MCM type OIP Package

- 40 x 40 x 6 mm (same as 304-pin QFP)
- 88 electrical pin
- Optical Connector (12 MT)

- Ceramic package
- Limiter amp
- MSM-OEIC
- LDD
- VCSEL
- Land for PQFP (SER/DES)
- P-WG
- MT receptacle
Implemented 1000BASE-SX

64 x 66 PCI
graphic card
OIP-LSI
NIC
MSM-OEIC output (RX)
TX optical output
@1.25 Gb/s

The ceramic package was expensive and assembly yield was low.
The optical interface should be assembled on other small substrate.

3. PETIT
Photonic and Electronic Tied InTerface
- BGA package with PETIT
- PETIT configuration
- link budget
- LDD in CMOS
- TIA
- Sub assembly, optics
- PETIT connector
- BGA substrate
BGA type OIP Package

- BGA substrate (35 x 35 mm, standard 352-pin)
- PETIT (8 x 8 mm)
- CMOS chip
- PETIT Fiber-connector

Cross sectional view:
- Heat sink
- Fiber connector
- PETIT
- CMOS
- BGA substrate
- Mold (if necessary)

All optical and analog chips are assembled on the ceramic substrate.
In-package optics − Mounting PETIT directly on a BGA substrate.

PETIT Configuration

12.5 Gbps full-duplex in 8 x 8 mm size

- AlN substrate (8 x 8 mm)
- TIA
- VCSEL
- PD

- 12.5 Gb/s full duplex
- 8 x 8 mm ceramic (AlN)
- P (typ) 1.2 W (Vdd 3.3 V)
- TX: 4 x 3.125 Gbps
- 850-nm VCSEL
- no LDD (included in CMOS)
- RX: 4 x 3.125 Gbps
- MSM-PD (GaAs)
- TIA (GaAs)
TX (LDD in CMOS and VCSEL)

CMOS: NEC’s UR2H (0.25 um)

similar circuit with OETC
(cf. T. C. Banwell, et. al. J. Quant. Electron. 29., 635, ’93)

(probe card: noisy, BW ~ 1.0 GHz)

RX (TIA (GaAs) and PD)

GaAs: NEC’s GES01 (0.2 um) CMOS: UR2H (0.25 um)

BW of the socket is ~ 1.5 GHz

RX output of PETIT
Optics
PETIT and PETIT connector

Commercial MT connector can be used.

4. CMOS

- Cross-point switch
- Multi channel SERDES
Cross Point Switch

3.125 Gb/s 16 x 16  NEC UR2H (0.25 um)

All high-speed signals are optically Input and output via PETIT

Multi Channel SERDES

4 x 3.125 Gb/s SERDES  NEC UR2H (0.25 um)

coded and multiplexed D0.0 (opt)  de-multiplexed and decoded 1,1,0,0
5. Library files
conventional cell-based ASIC design flow

CMOS chip
- Core logic
- Soft IP (codec) (deskew)
- Hard IP (SERDES) (LDD, amp)

BGA package
- PETIT

HDL
- TLF
- UDL
- PADLIB

6. HDTV Switcher

- Block diagram
- PWB, lack
Demonstrating 10-Gb/s interconnection and compact implementation.

Y, Pb, Pr elemental signals are modulated

PWB, Lack
800-Gbps-I/O / board

365 x 270 mm
7. Summary

(1) We developed OIP

(2) PETIT realized 12.5 Gb/s duplex optical interface in 8 x 8 mm.

(3) 100 Gb/s optical I/O chip was developed by using OIP.

I/O 64 Gb/s 430 x 540 mm

I/O 800 Gb/s 365 x 270 mm

I/O 100 Gb/s 35 x 35 mm

Acknowledgements

Tetsuya Yamazaki, Osamu Matsuo, Yuji Akimoto, Watanabe, and Shigeo Sato
R&D Support Center, NEC

Mitsuru Kurihara
Product Technology Research Laboratories, NEC

Shunji Doi
PWB Division, NEC Electron Devices

Jun Kato
NEC Tohoku

Hideki Tanaka, Takumi Dohmae, and Masami Nanba
NEC Engineering

Tetsuya Enomoto
NSW