160Gb/s Serial Line Rates in a Monolithic Optoelectronic Multistage Interconnection Network

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Outline

• Nanosecond-timescale reconfigurable interconnection
  – State of the art using III-V technology
  – Scaling optoelectronic circuits

• Experiment
  – Circuit fabrication
  – Optical multiplexing
  – Ultrahigh speed serial routing

• Conclusions and prospects
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Ultrafast photonic interconnects

Data Vortex at Columbia University

OSMOSIS program with IBM and Corning

- Tens of connections at tens of Gigabit/s per connection
- Ultrafast nanosecond reconfiguration with III-V switch technology

- Pros for III-V semiconductor optical amplifier gates
  - Fast switching, ease of electrical control, massive bandwidth
- Cons: complex implementation using discrete photonic parts
  - Packaging dominates cost, energy losses, time delays, control

A need for photonic integration
Progress in photonic integration

1970
1980
1990
2000
2010
Integrated photonic interconnects

- Integrated photonics proposed for a broad range of interconnections
  - on-chip wiring
  - on-board wiring
  - backplanes
  - routers
  - telco
- Point to point parallel optics through to wavelength managed busses
- Focus here on optoelectronic switching
  - decouple bandwidth and energy use
  - broadband (multi-Terahertz) fabrics
  - low intrinsic delay and latency
  - scalable with intrinsic gain

HOTI - 2008, Beausoleil, HP

courtesy IBM Zurich

University of Cambridge
Switch circuits

- Range of circuits proposed with varying degree of fabrication complexity and tolerancing
- Crosstalk improved for non-interferometric switch solutions
- Limited data on high data rate transmission and routing
Switch circuits

- Scaling so far to 4 inputs 4 outputs with crossbar and broadcast architectures
  - Serial line rates at 10Gb/s
  - Signal degradation in ICs
  - Architectures scaling poorly
- Monolithic multistage interconnection networks offering route to higher connections
Multistage Interconnection

- Clos/broadcast&select hybrid network
- Trade off between number of stages and connection scaling
- 16x16 switch architecture demonstrated with 4x4 fabrics at $8\lambda\times10\text{Gb/s}$ with just 3.4dB penalty

_H. Wang et al., Optical Fibre Conference, 2009_
Monolithic multistage interconnect

- Levels of complexity increasing in current generation of integrated switching circuits
- Low power penalty (signal degradation)
  - 0.2dB for single stage, 0.5dB for two stages
  - negligible crosstalk penalty
- Good power penalty performance, but unclear what the physical limits are

A. Mejia et al., Optical Fibre Conference, 2009
Scaling limits in photonics

Numerical study into scaling

Mixed time and frequency domain modelling allowing a mapping of low signal degradation

Technique scanned to map large connectivity networks at 100Gb/s

Williams et al., NuSOD Post Deadline, 2008
Scaling connectivity

- 3 stage network with 2dB power penalty for 64x64 at 100Gb/s/path
- Motivation for further study into bandwidth versus number of stages
- BUT WDM complexity becoming considerable
  - of interest to also scale serial line rate (as in telco)

*Williams, K.A. et al, NUSOD, Post-deadline ThPD5 (2008)*

Scaling capacity

• Power efficiency in photonics derived primarily from intrinsic massive bandwidth (tens of Terahertz)

• Optical multiplexing techniques allowing aggregation of electronic lanes but ...

• Dense wavelength multiplexing carries a management overhead:
  • Strict wavelength registration across the photonic network
  • Strict thermal management
  • Multiple power consuming transmitters

• Serial transmission for reduced hardware and management complexity
  • High serial line rates so far unproven for integrated photonics
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Monolithic optoelectronic circuit

- Active passive regrown wafer process on InGaAsP/InP

Circuit fabricated at TU Eindhoven through the JePPIX Multi Project Wafer platform
www.jeppix.eu
Monolithic optoelectronic circuit

- Active epitaxial layer stack for switch elements
- Passive epitaxial layer stack for waveguide routing
Active-passive regrowth: I

- Starting wafer includes InP substrate and InGaAsP active layer
- Active islands defined photolithographically
- Mask layers not shown for clarity
Active-passive regrowth: II

Active layer stack selectively removed
Active-passive regrowth: III

Confinement layer infilled with no active quantum wells
Active-passive regrowth: IV

- Arrays of active fingers of area 30 microns by 1000 microns formed across a regrown 2" wafer
- Technique commercially deployed for high end transceivers
Active-passive crossbar

- Full circuit comprised of six crossbars
- 1mm² circuit area per crossbar in current generation
- Circuit area reduced for a given wafer topology by co-locating gates

Orthogonal waveguide crossings for low crosstalk

Two gates per active island for increased circuit density

Planar waveguide splitters for fabrication resilience
Waveguide design

- Deep etch waveguides for tight bend radius (0.1mm) photonic wiring
- Shallow etch waveguides for amplifiers gates and waveguide crossings
- Two amplifiers per electrode

Waveguide top view

Waveguide cross-sections

- Deep passive
- Shallow active
- Shallow passive

Bar state
1 ↔ 1'
2 ↔ 2'

Cross state
1 ↔ 2'
2 ↔ 1'
Circuit

- 4 input 4 output crossbar switch network implemented in four stages
- Network readily scalable to higher connectivity
- Input to output combination determines number of crossbars in path
- Exploits repeatable cell design
• Constraints from first generation regrown wafer required folding of circuit
• On-chip gain readily achieved - deduced from oscillations from uncoated facets - biased below oscillation point in this work
• 10 of 16 paths functional (mask error and short circuit restricts full function)
• Shortest and longest paths through two stages of crossbar and four stages of crossbar
160Gb/s experimental testbed

Transmitter

+7dBm aggregate power in fibre

Circuit under test

in separate lab

Fibre to chip coupling loss estimated at 6dB
Time division multiplexing

- Pseudo random sequence generated directly at 40Gb/s
- Time interleaved with half sequence delays to generate true PRBS at 160Gb/s
Time division demultiplexing ÷ 4

- Test approach deployed sequentially tests interleaved tributary channels
- Full test schemes for both multiplexing and demultiplexing feasible through parallel optoelectronics at 40Gb/s
Bit error rate: 40Gb/s

Power penalty used as a metric of system degradation

Logarithmic relation indicates noise limited
Bit error rate: 160 Gb/s

- Increase in penalty with stage number attributable to noise build up
- Increase in penalty with line rate attributable to increased aggregate power
- Both may be reduced though circuit loss reduction
160Gb/s time averaged time traces

- Eye diagrams observed through an optical sampling front end to an electronic oscilloscope (Agilent Terascope)
- Clear eye opening for input signal and signals after two and four stages
160Gb/s time averaged spectra

Time averaged spectra with limited spectral evolution

5nm spectral width not yet exploiting the tens of nanometres bandwidth potentially available

160Gb/s x 4 paths = 3pJ/bit for crossbars

0.3W x 6 crossbars
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Conclusions and prospects

- Demonstration of monolithically integrated four stage photonic integrated circuit
- Scalable architecture
  - additional connections feasible through additional crossbars
  - route to lossless switching
  - additional unused bandwidth for no additional energy cost
- First demonstration of 160Gb/s serial routing through optoelectronic crossbars
  - 1.3dB power penalty for 4 stages
- Route towards massive bandwidth density integrated photonic signal processing

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