

The international forum where the high-performance computing and high-speed networking communities meet

## Join us on the Google campus for Hot Interconnects 2010!

Building on last year's successful keynote, session, and panel on Wall Street's challenges, requirements, and solutions, in 2010 Hot Interconnects moves to Google campus, Mountain View, CA for the conference. We hope you can join us there.

Hot Interconnects is the premier international forum for researchers and developers of state-of-the-art hardware and software architectures and implementations for interconnection networks of all scales, ranging from multi-core on-chip interconnects to those within systems, clusters, and data centers. Leaders in industry and academia attend the conference to interact with individuals at the forefront of this field.

Themes include cross-cutting issues spanning computer systems, networking technologies, and communication protocols. This conference is directed particularly at new and exciting technology and product innovations. Contributions should focus on real experimental systems, prototypes, or leading-edge products and their performance evaluation. In addition to those subscribing to the main theme of the conference, contributions are also solicited in the topics listed below.

### CALL FOR PAPERS

- Novel and innovative interconnect architectures
- Multi-core processor interconnects
- System-on-Chip Interconnects
- Advanced chip-to-chip communication technologies
- Optical interconnects
- Protocol and interfaces for interprocessor communication
- Survivability and fault-tolerance of interconnects
- High-speed packet processing engines and network processors
- System and storage area network architectures and protocols
- High-performance host-network interface architectures
- High-bandwidth and low-latency I/O
- Tb/s switching and routing technologies
- Innovative architectures for supporting collective communication
- Novel communication architectures to support grid computing
- Requirements driving high-performance interconnects
- Traffic characterization for HPC systems and commercial data centers

#### Submission Guideline

- **Submission deadline: April 25, 2010**
- Notification of acceptance: June 6, 2010
- Papers need sufficient technical detail to judge quality and suitability for presentation. Paper limit: 8 pages, two column.
- Submit title, author, abstract, and full paper (eight pages, double-column, IEEE format).
- Papers should be submitted electronically to:  
<http://www.easychair.org/conferences/?conf=hoti2010>
- For further information please see <http://www.hoti.org>

#### About the Conference

- Conference held at Google campus in Mountain View CA.
- Papers selected will be published in proceedings by the IEEE Computer Society.
- Presentations are 30-minute talks in a single-track format.
- Online information at <http://www.hoti.org>.

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