Intel® QuickPath Interconnect
Architectural Features Supporting Scalable System Architectures

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Agenda

• Overview
• Scalability
• Error Handling
• Future Extensions
Intel® QuickPath Interconnect

- High speed, packetized, point to point, coherent system interconnect
  - Handles two socket servers and up
  - Architecture built for scaling efficiently
  - RAS features to support large systems

- Layered Architecture
  - Modularity & Flexibility
  - Rich Link layer features
    - MCs and Virtual Networks
  - Coherent and Non-Coherent Protocols
  - Applied to both Intel® Xeon® and Itanium® processor based systems
Typical Platform Topologies

2 socket server

8 socket server

4 socket server

- Multiple distributed memory controllers
- Platform wide coherency protocol
- Routing functions for message delivery
- Flexible configurations
Very Large Systems

Up to 8 Sockets: Node Controllers Optional
Larger than 8 sockets: Node Controllers Required

EX = Intel® Xeon processor 7500 series
Intel® QPI Features for Scalable Systems

• MESIF Coherency Protocol
  – F State => Clean line forwarding
  – Single round-trip delay for cached data

• SADs, TADs, and RTs
  – SADs determine where to send request
    – Socket interleaving
  – TADs determine who gets it
    – Memory Channel interleaving
  – RTs determine how it gets there
    – Local socket, or out another link
  – Configuration done through firmware at boot
  – Can be tailored to NUMA or UMA configurations
SADs and TADs - Interleaving

SAD Conceptual Diagram

Physical Address

Socket Interleaving Example

Attributes  Destination Node ID

IEEE Hot Interconnects 2010
SADs and TADs - Interleaving

Channel Interleaving Example

Destination NodeID
Attributes
TADs
Targeted Function

Socket 1 Memory

Ch0 Ch1 Ch2

CPU A
Home Cache

Socket 2 Memory

Ch0 Ch1 Ch2

CPU B
Cache Home

IOH

System Memory Map

IEEE Hot Interconnects 2010
Efficient Bandwidth Utilization

• Variable length messages
  – All messages built from one or more ‘Flits’
  – Most common messages are encoded into shortest format

• Source snoopy protocol
  – Good for transaction processing, 2-8 sockets

• Minimizing the number of messages
  – Source snoop and/or directory controlled caching agents
  – No need to send snoops to the home agent getting the request
  – Multiple caching and home agents in a single socket
  – Router broadcast of snoops
Reliability in Scalable Systems

- Routing layer allows system partitioning to smaller clusters for application isolation & reliability
- System reconfiguration without bringing the system down
- Intel® QPI also allows memory writes and reads to be mirrored
Error Handling

• Detection
  – All messages built from 80 bit Flits
  – 8 bits of CRC in every Flit
  – Optional 16 bit rolling CRC

• Recovery
  – Link layer retry process
  – Link in-band reset on too many failed retries

• Reduce single points of failure
  – Link reconfiguration on data lane failure
  – Link reconfiguration can also substitute for a failed clock using one of the data lanes

• Poison and Viral Responses
Future Extensions

• Increase speed on the link
  – Similar to FSB history, growth in transfer rates over time

• Improve Power Management
  – Integrated into the overall CPU and platform power management policies

• Improve messaging efficiency
  – In terms of link utilization or latency
  – Reduced implementation and validation complexity
Summary

• Looked at basic Intel® QPI functions and topologies
• Described some scalability features
• Reviewed Intel® QPI RAS Features
• Touched on the future
THANK YOU!

Q&A
Additional sources of information on Intel® QuickPath Interconnect:

- Web info:

- Books: Published by Intel Press

  **Weaving High Performance Multiprocessor Fabric**
  Architectural Insights into the Intel® QuickPath Interconnect
  By Robert A. Maddox, Gurbir Singh and Robert J. Safranek

  **Mastering High Performance Multiprocessor Signaling**
  Electrical Design with the Intel® QuickPath Interconnect
  By Dave Coleman, Michael Mirmak