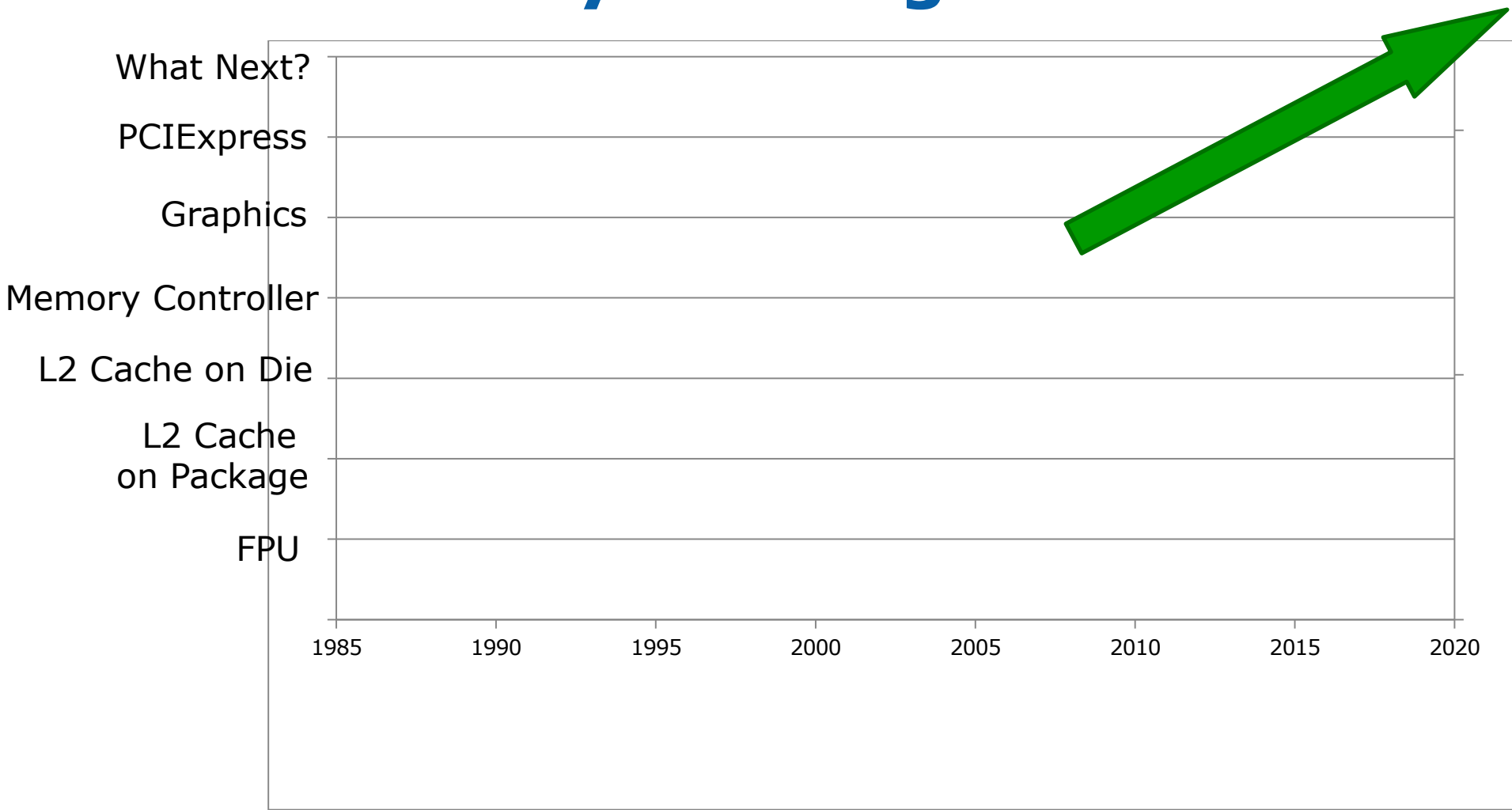


The March of Moore's Law: Driving System Scale Integration

Keith D. Underwood



The History of Computers is a History of Integration



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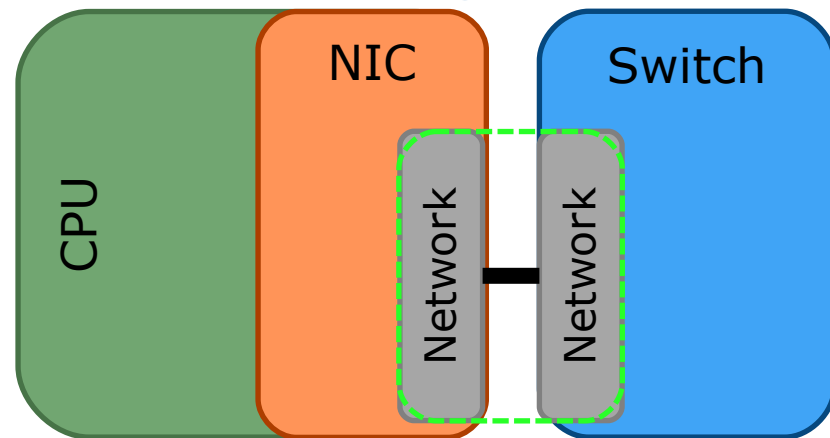
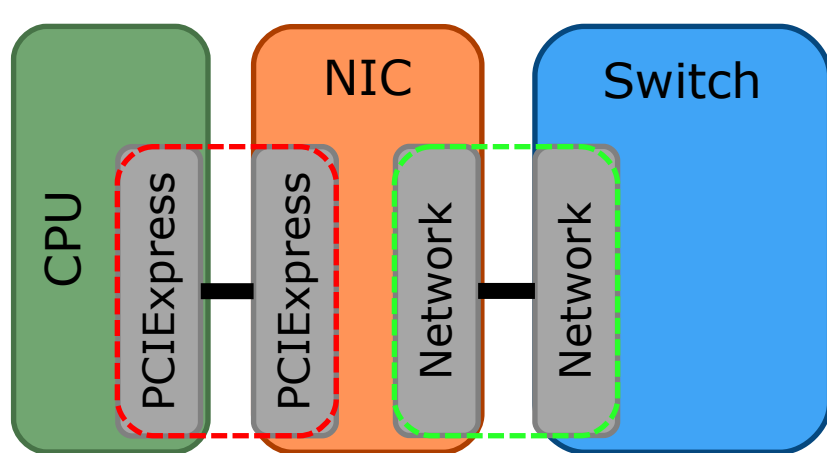
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What Next for Integration?

For HPC: It should be the Network



Discrete NIC creates Challenges:

- PCIExpress*
 - Designed for commodity board infrastructure
 - Low demand for bandwidth improvement in volume space – 8 Gb/s today
 - Semantics designed for broad adapter ecosystem
- Adds electrical interface that
 - Adds power
 - Adds latency

Integrating NIC creates Advantages for HPC:

- Exports native network link
 - Engineered for high performance electrical channel
 - High demand for bandwidth improvement – 14 Gb/s today
 - Provides native HPC semantics
- Eliminates redundant link to CPU (reduces power, reduces latency, improves MTBF)
- Enables “real” remote atomics

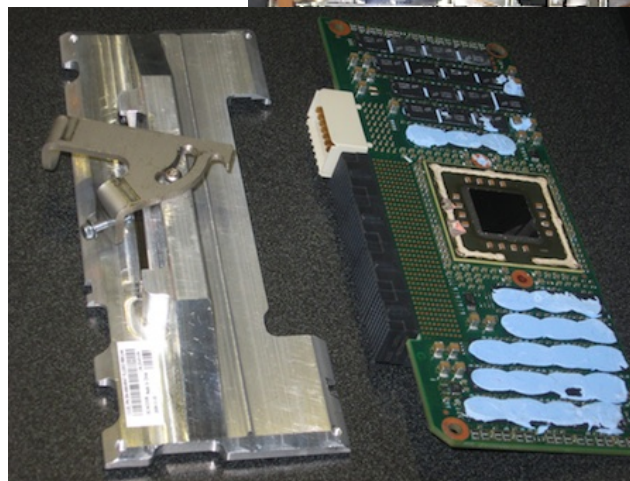
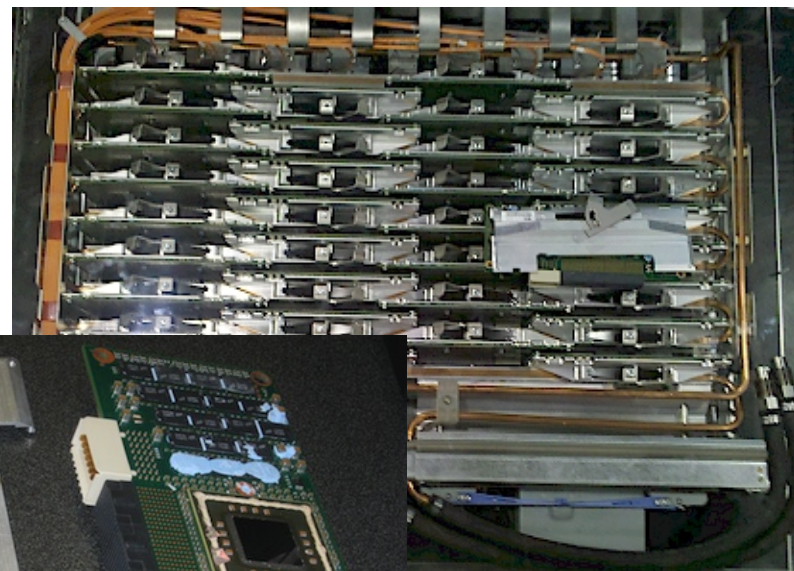
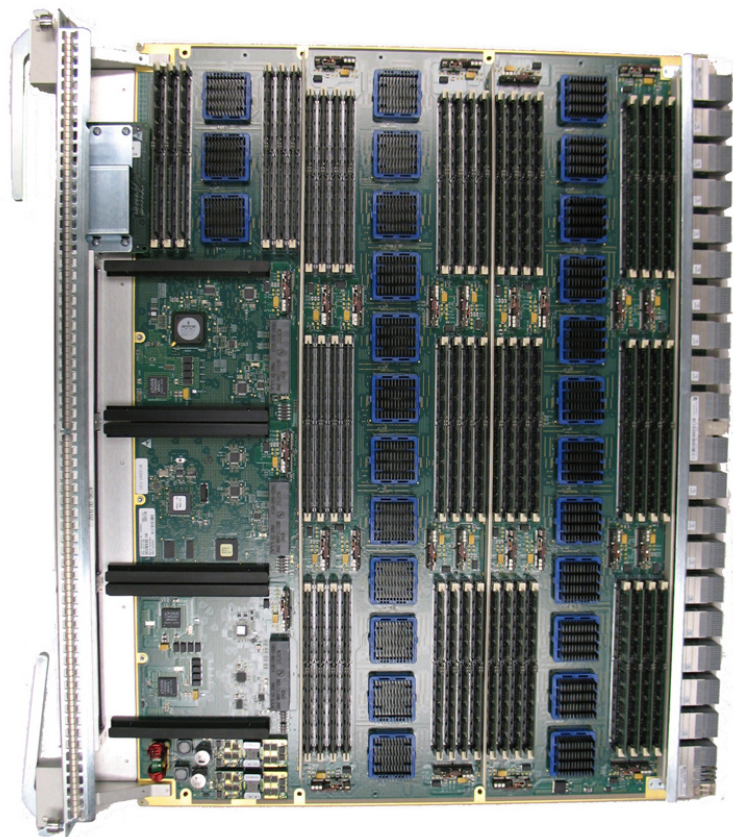
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A Form Factor Opportunity



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Challenges Facing the Integration of an HPC Network

- What to integrate?
 - Mobile: Wireless!
 - Server: Ethernet!
 - HPC: Something Useful!
- Platform Challenge: high speed signaling exiting a CPU socket
- Product cycles
 - HPC networks happen every 3 years (or so)
 - Must sell enough to match cost of development
 - Basic technology (signaling, cabling, optics, boards) does not change any faster

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CPU platforms change every 2 year

Lack of alignment is a business challenge!

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Summary

- Improving transistor density has repeatedly drawn more system components on die to deliver superior products
- HPC would exploit integration of the network for significant gains
 - Improved bandwidth off-package
 - Improved system level form factor
 - Reduced power
 - Improved semantics
- Biggest challenge facing network integration: wildly divergent requirements

HPC has not traditionally wanted Ethernet

Most capable HPC networks may be harder to exploit in other usage models

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