A Low Latency Library in FPGA Hardware for High Frequency Trading (HFT)

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August 22, 2012, Santa Clara, CA
Outline

• Introduction
  – High Frequency Trading (HFT)

• Survey of HFT Platforms
  – Software, Hardware, and Hybrid Approaches

• Field Programmable Gate Arrays (FPGAs)
  – Advantages and Disadvantages

• Algo-Logic’s Low Latency Library
  – Implementation on NetFPGA 10G Platform
  – Exposure and Position Tracking Application
  – Protocols Supported

• Results
High Frequency Trading (HFT)

• **HFT is**
  – Trading of equities, options, futures at high speed in large volumes
  – Earning money by exploiting the fleeting variation in stock price or demand

• **HFT accounts**
  – 70% of all trades in US Markets in 2010
  – And it continues to grow

• **HFT involves**
  – Using computers to place orders based on pre-defined algorithms
Challenges in Financial Markets

Main Challenges

• **Latency**
  – Execute orders faster than other investors to capture fleeting variations in price and demand in the markets

• **Jitter**
  – Provide consistent and fair executions

Secondary challenges

• **Throughput**
  – Handle large volume of orders

• **Flexibility**
  – Adapt to changing risks and trading strategies
Recent Problems in HFT

• **Knightmare (Knight Capital)**
  – Test script executed live trades
  – $450M loss in 45 minutes

• **Nasdaq - Facebook IPO**
  – Order confirmations delayed
  – $62M loss in direct damages

• **BATS Failure**
  – Software bug in order auctions
  – Forced to cancel IPO

Have not only hurt the banks/institutions financially, but also the credibility of the market
Latency in Current Approaches

Software

- **Linux 10GE NICs**
  - 15-20 µs for Half-Round Trip Time (½ RTT) through un-optimized kernel
  - TCP Offload: 2.9 µs Transmit + 6 µs Receive for ½ RTT

- ** Datagram Bypass Layer (DBL)**
  - 3.5 µs for UDP and 4.0 µs for TCP

- **Infiniband MPI**
  - 1 µs (excluding application layer)

Hardware

- **Graphics Processor (GPU)**
  - Optimized for throughput, but not optimized for low latency
  - Incurs additional overhead of passing data through PCIe bus

- **ASIC**
  - Achieves sub-µs latency
  - But lacks flexibility to handle new protocols and features

- **FPGA**
  - Provides 0.2 µs latency w/TCP
  - Has the flexibility to support new protocols and features
FPGA Approaches

Hybrid Computing
CPU + NIC + FPGA Offload

- Unpredictable PCIe bus transfer
- Memory copy
- Potential cache misses
- Amdahl’s law

Pure FPGA Computing
FPGA handles all computing

- No bus copy
- No memory copy
- No cache misses
- Parallel execution
FPGA outperforms Software

Latency
- Hardware: 0.2 μs
- Software: 5 μs

Jitter
- Hardware: 6 ns
- Software: 600 ns
• Software solutions
  – Require less development time to get started
• But FPGA hardware solutions achieve lower latency
  – That fundamentally cannot be achieved with software
Algo-Logic’s Low Latency Library

- Infrastructure
- Protocol Parsers
- Market data in local memory

[Diagram of Algo-Logic Platform]

- Host PC
- Host Application
- Algo-Logic C++ API
  - Networking Stack
  - OS Kernel
- Physical Layer
  - NIC
  - PHY
- Data Link Layer
  - 10G MAC
- Network Layer
  - 10G Ethernet Links
  - Host (UDP)
  - Broker
  - Exchange
- Application Layer
  - Stock Price Tables
  - Application Layer (Custom Logic)
  - Financial Protocol Parser
    - Session
    - Datagram
    - IP Processing
  - FPGA
  - SRAM Controller
  - QDR II SRAM
- Market data in local memory
- Infrastructure
- Protocol Parsers
Protocol Parsers

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**Algo-Logic Platform**
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- Application Layer (Custom Logic)
  - Financial Protocol Parser
  - Register Interface
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- Datagram
- IP Processing
- FPGA
- 10G MAC
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- μBlaze Soft CPU
- SRAM Controller
- QDR II SRAM

**Physical Layer**
- NIC
- PHY

**Data Link Layer**
- 10G Ethernet Links

**Network Layer**
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**Application Layer**
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**Networks**
- FIX
- Financial Information eXchange
- OUCH
- NASDAQ
- XPRS
- DirectEdge
- BOE
- BATS BZX
- ArcaDirect
- NYSE Arca
- Native Trading Gateway
- LSE
View of an Nasdaq order in the FPGA

OUCH Packet Data

“O” = OUCH Enter Order Message
14-byte Order Token
Buy/Sell Indicator
Number of Shares
Stock Name
Price
Market Data and On-chip Storage

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Physical Layer

Data Link Layer
- 10G MAC

Network Layer
- Networking Stack
- OS Kernel

Application Layer
- Host Application
- Algo-Logic C++ API
- Networking Stack

Host (UDP)

10G Ethernet Links

Broker

Exchange
• Starting with a pre-built low-latency library
  – Reduces the initial development effort
• But maintains fundamental benefits of FPGA solution
  – Full data-path remains in low-latency hardware
Areas of Application

Algo-Logic’s Low Latency Libraries provide lowest latency for **Traders**, **Brokers**, **Market Makers** and **Exchanges** in the areas of:

- **Trading Strategy**
- **Internalization**
- **Feed Processing**
- **Smart Order Routing**
- **Risk Management**
- **Matching**
Operations performed in hardware

- Parsing FIX execution reports
- Update price per Security to calculate
  - Long Exposure
  - Short Exposure
  - Value/Security (across all sessions)
  - Position/Security (across all sessions)
- Sending these values to the customer
  - On a programmed, periodic basis
Example: Position & Exposure Monitor

- Market Data
- UDP Logs
- FIX Orders
- NetFPGA 10G
- 10Gbps Ethernet Links
- Latency (<2μs)
- Exchange/ECN
- FIX Execution Report
## Specifications & Performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value (demo)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware platform</td>
<td>NetFPGA-10G</td>
</tr>
<tr>
<td>Application</td>
<td>Position &amp; Exposure calculation</td>
</tr>
<tr>
<td>Protocol</td>
<td>FIX 4.2</td>
</tr>
<tr>
<td># sessions supported</td>
<td>10</td>
</tr>
<tr>
<td># securities supported</td>
<td>100</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>Line rate, 10 Gbps</td>
</tr>
<tr>
<td>Latency (Logic processing inside FPGA)</td>
<td>200ns</td>
</tr>
<tr>
<td>10GbE PHY delay</td>
<td>400ns (one-way)</td>
</tr>
<tr>
<td>Total Latency (pin-to-pin)</td>
<td>1µs</td>
</tr>
</tbody>
</table>
Results

• **Low latency library**
  – Implemented as FPGA gateware

• **Implements**
  – Order flow processing infrastructure
  – Protocol parsing for all major exchanges
  – Maintains market data in local memory

• **Demonstrated**
  – Ten sessions of FIX 4.2 on NetFPGA 10G

• **Achieves**
  – Jitter-free processing with 200ns latency
More about Accelerated Finance

Algo-Logic builds high frequency trading solutions that have the lowest delay and time variation bounds possible. By implementing order processing algorithms in FPGA hardware, sub-microsecond (μs) processing delays with only nanoseconds (ns) of time variation is achieved, which is impossible to obtain in software. Algo-Logic offers:

- Finance protocol parsing libraries with support for FIX, OUCH, XPRS, ArcaDirect, BOE, and LSE
- Pre-built infrastructure for reduced time to market

**Key Benefits**

- The lowest latency possible is achieved by parsing in FPGA hardware
- Deterministic performance eliminates order processing time variations
- UDP/IP-based control and monitoring interface makes operation of the hardware easy from graphical and command line interfaces
- Line rate processing at 10 Gigabits/second

[Contact us](#) to get more information