Enhanced Overloaded CDMA Interconnect (OCI) Bus Architecture for on-Chip Communication

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HOTI, 2015
Outline

1. Background
   - From T/SDMA to CDMA
   - Conventional On-Chip CDMA Bus

2. Overloaded CDMA Interconnect (OCI)
   - Pair difference codes
   - Proposed Bus Architecture

3. Results
   - T/SDMA vs CMDA
   - Performance

4. OCI vs AXI
   - High Level Synthesis (HLS) OCI Bus
   - D-OCI vs AXI results

5. Conclusions and Future Work
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5. **Conclusions and Future Work**
Time Division Multiple Access (TDMA)

- In TDMA: Bus access is time shared.
- Arbitration overhead increases with the number of cores.
- Capacity is limited by the number of time slots.
Space Division Multiple Access (SDMA)

- In SDMA: point to point connection by crossbars.
- Best connectivity at the expense of quadratic complexity.
- Capacity is limited by the complexity.
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Code Division Multiple Access (CDMA)

- In CDMA: Bus access is code shared.
- Each core has a unique N chip spreading code
- The data from each core is spread by XORing the data with each chip in the spreading code.
- The spreading codes are summed and sent serially on the bus.
- Data can be extracted from the bus by correlating with the signature code.
- CDMA requires a single user receiver (Matched filter).
Conventional CDMA bus

- Data is XORed with the spreading code.
- All spreading codes are summed.
- Correlation is done using two accumulators.
- The accumulator with the larger value determines the sent bit.

![Diagram of Conventional CDMA bus](image)
Why CDMA for On-Chip Interconnects?

- CDMA for on-chip interconnects is not fully explored yet, leaving a room for optimization.
- As shown in this paper, the bus capacity and bandwidth can be easily increased by applying some new innovative ideas.
- In this work, we aim to increase the capacity without increasing the complexity.
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Non-Orthogonal Pair Difference (PD) codes

- In the orthogonal code set, the difference between two consecutive bus sums is always even, we call it the pair difference (PD).
- Non-orthogonal codes can be added on the bus that alters the modulo 2 of PD.
- The modulo 2 of PD can thus determine the data encoded in the non-orthogonal code.
For a spreading code set of length $N$ chips, there are only $N/2$ pairs of chips.
Therefore, there can exist only $N/2$ PD codes.
The codes can be generated by the formula $PD[l] = 2^{7-2l}$, $0 \leq l < N/2$.

\[
PD[0] = 2^7 = \{1, 0, 0, 0, 0, 0, 0, 0\} \\
PD[1] = 2^5 = \{0, 0, 1, 0, 0, 0, 0, 0\} \\
PD[2] = 2^3 = \{0, 0, 0, 0, 1, 0, 0, 0\} \\
PD[3] = 2^1 = \{0, 0, 0, 0, 0, 1, 0\}
\]
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Overloaded CDMA Bus
We propose an overloaded CDMA architecture based on the PD codes, thus called the Difference-OCI (D-OCI).

- Full capacity bus implemented on AC701 FPGA kit.
- Two architectures are implemented: reference and pipelined architectures.
Hybrid Encoder

Bus Controller

Encoder wrapper for IP core 1

Encoder wrapper for IP core M

Encoded Data Register

Arithmetic Adder

Sum Register

Bit-Slice A-1

Bit-Slice 0

Decoder wrapper for an IP core using an orthogonal code

Orthogonal Decoder 1

Orthogonal Decoder 2

Decoder wrapper for IP cores using PD codes

1x2 Shift Register

Reg[0]

Reg[1]

Reg[N]

Reg[N-1]

1xN Shift Register

Reg[N]

Memory/Peripheral 1

Memory/Peripheral 2

Memory/Peripheral N

Memory/Peripheral 1.5 N
Hybrid Encoder

- The encoder is AND gate.
- If data is 0 send a stream of 0, the pair difference remains even.
- If data is 1 send a non-orthogonal PD code causes the pair difference to be odd.
- The modulo 2 of the pair difference is detectable.
Binary Bus Adder

- Adds the encoded chips from all encoders.
- The sum produced by the adder is passed to all decoders.
- Surrounded by two pipeline register isolating the critical path in the adder.
Decoders

Bus Controller

Counter

To All Code Generators

start

idle

Bit-Slice A-1

Bit-Slice 0

Encoder wrapper for IP core 1

Hybrid Encoder 1

Spreading Code Gen

Orthogonal Mux

PDs

Encoded Data Register

Arithmetic Adder

Binary Signaling

m-bit width

Sum Register

Orthogonal Decoder 1

Zero Accumulator

One Accumulator

Despreading Code Gen

Orthogonal Decoder 2

1x2 Shift Register

Reg(0)

1xN Shift Register

Reg(N)

Reg(N-1)

Decoder wrapper for IP cores using PD codes

Memory/Peripheral N-1

Memory/Peripheral N-1.5

Memory/Peripheral data

despreading code config

ip core 2

...​

ip core M

A-bit width

ip core 1 data

spreading code config

start idle

ack valid

results

oci vs axi

conclusions and future work

background

overloaded CDMA interconnect (oci)
Decoders

- The orthogonal code decoders resemble the decoder employed in conventional CDMA.
- The PD code decoders employ an XOR gate to determine the modulo 2 of the pair difference.
- The inputs to the XOR gate are the LSBs of the bus sums in a pair.
- A register is used to hold the incoming LSBs of the bus sum.
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T/SDMA vs CMDA

(a) Resources as combinational (hashed) and non-combinational (solid) in LUT-FF

(b) Maximum bus frequency in MHz

(c) Log scaled bus bandwidth in Mbps

(d) Dynamic power decipated in mW

[Graphs showing comparisons for each category]
T/SDMA vs CMDA

- Conventional CDMA utilizes a higher area than TDMA but offers equivalent bandwidth.
- Conventional CDMA provides lower bandwidth than SDMA but consumes much smaller area.
- OCI bus can improve the bandwidth and reduce the area per IP core.
- We compare the conventional CDMA to T/SDMA, we then compare the D-OCI the conventional CDMA along with the M-OCI developed in our previous work.
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</table>
Area

- Number of IPs is 50% more.
- The extra area is small compared to extra IPs.
- Area per IP is reduced.
Frequency

- Computation path is increased.
- The maximum frequency decreased.
- Can be fixed by pipelining the bus adder.

![Graph showing Frequency vs Number of Chips]

- Conventional
- M-OCI
- D-OCI
- D-OCI Pipelined
Bandwidth

- The number of sent bits increased by 50%.
- Bandwidth increased.
Power Consumption

- Area per IP is reduced.
- So power per IP is reduced.

![Graph showing power consumption vs number of chips for different interconnect types: Conventional, M-OCI, D-OCI, D-OCI Pipelined. The graph indicates that power consumption decreases as the number of chips increases for all interconnect types.](image-url)
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HLS OCI Bus

- The AXI bus is widely deployment in modern SoCs, it is extensively supported by different vendors and CAD tools and supports both TDMA and SDMA bus access.
- To compare the OCI to the AXI, we implemented a D-OCI HLS IP using the Vivado HLS tool.
- OCI and AXI implemented and validated on the Zedboard Zynq-7000 SoC
OCI vs AXI testbed
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## D-OCI vs AXI results

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<tr>
<th>Bus Topology</th>
<th>Bus Capacity (M \times M)</th>
<th>LUTs</th>
<th>FFs</th>
<th>Latency clock cycles</th>
<th>Frequency MHz</th>
<th>Bandwidth Gbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>D-OCI N = 8</td>
<td>11 \times 11</td>
<td>177</td>
<td>222</td>
<td>13</td>
<td>109</td>
<td>2.951</td>
</tr>
<tr>
<td>D-OCI N = 16</td>
<td>23 \times 23</td>
<td>487</td>
<td>567</td>
<td>22</td>
<td>113</td>
<td>3.78</td>
</tr>
<tr>
<td>AXI SAMD-Crossbar</td>
<td>11 \times 11</td>
<td>8,229</td>
<td>5,651</td>
<td>42</td>
<td>104</td>
<td>0.871</td>
</tr>
<tr>
<td>AXI SAMD-Crossbar</td>
<td>16 \times 16</td>
<td>11,299</td>
<td>7,833</td>
<td>61</td>
<td>93</td>
<td>0.78</td>
</tr>
<tr>
<td>AXI SASD-TDMA</td>
<td>11 \times 11</td>
<td>2,123</td>
<td>1,761</td>
<td>122</td>
<td>107</td>
<td>0.309</td>
</tr>
<tr>
<td>AXI SASD-TDMA</td>
<td>16 \times 16</td>
<td>2,919</td>
<td>2,532</td>
<td>177</td>
<td>105</td>
<td>0.304</td>
</tr>
</tbody>
</table>
D-OCI vs AXI results

- The D-OCI bus contains only the write channel while the AXI contains read, write and write response channels.
- This causes the magnitude difference in utilization of the D-OCI bus over AXI Shared Address Shared Data (SASD) bus.
- D-OCI demonstrates the lowest latency since addressing the slaves is done once before the data transaction.
- AXI Shared Address Multiple Data (SAMD) demonstrates higher transaction latency than the D-OCI since the addressing is done in sequence.
- AXI SAMD should demonstrate lower latency than the D-OCI in burst access mode.
Conclusions

- On-Chip CDMA is not fully explored yet.
- CDMA capacity can be boosted by 50% using orthogonal signature code properties.
- The OCI can be used as the core interconnect of buses and NoCs.
Future Work

- Architectural enhancements: pipelining, resource sharing.
- Explore more signature code properties.
Thank You