

The international forum where the high-performance computing and high-speed networking communities meet

MONDAY, AUGUST 28

TRACK 1	Tutorial 1 8:30 – 12:00	Exploiting High-Performance Interconnects to Accelerate Big Data Processing with Hadoop, Spark, Memcached, and gRPC/TensorFlow <i>D. K. Panda & X. Lu, Ohio State University</i>
	Tutorial 2 13:30 – 17:00	High Performance Distributed Deep Learning for Dummies <i>D. K. Panda, A. A. Awan, and H. Subramoni, Ohio State University</i>
TRACK 2	Tutorial 3 8:30 – 10:00	Designing and Developing Performance Portable Network Codes <i>P. Shamis, ARM & Y. Itigin, Mellanox Technologies</i>
	Tutorial 4 10:30 – 12:00	Developing to Open Fabrics Interfaces libfabric <i>S. Hefty, Intel & J. Swaro, Cray</i>
	Tutorial 5 13:30 – 17:00	The TraceR/CODES Framework for Application Simulations on HPC Networks <i>N. Jain, LLNL & M. Mubarak, ANL</i>

TUESDAY, AUGUST 29

MORNING	Welcome Address 9:00 – 9:10	<i>Elisabetta Romano, Ericsson</i>
	Keynote 9:10 – 10:15	RDMA deployments: from cloud computing to machine learning <i>Chuanxiong Guo, MSR</i>
	Best Papers 10:30 – 12:00	<ul style="list-style-type: none"> Improving Non-Minimal and Adaptive Routing Algorithms in Slim Fly Networks Routing Keys Fast Networks and Slow Memories: A Mechanism for Mitigating Bandwidth Mismatches
AFTERNOON	Large Scale Networking 13:00 – 14:00	<ul style="list-style-type: none"> WaveLight: A Monolithic Low Latency Silicon-Photonics Communication Platform for the next generation Disaggregated Cloud Data Centers An FPGA Platform for Hyperscalers Throughput Models of Interconnection Networks: the Good, the Bad, and the Ugly
	Invited Talk 14:00 – 14:45	Performance Isolation for Highly Efficient Shared Infrastructure Services <i>Nandita Dukkkipati, Google</i>
	Panel 15:05 – 16:35	Ethernet vs. HPC: Can the hyperscale Ethernet data center handle all workloads? Moderator: <i>Roy Chua, Partner, SDxCentral & Wiretap Ventures</i> <i>Yogesh Bhatt, Senior Director, Ecosystem Innovation & Strategy, Ericsson</i> <i>Dave Cohen, Senior Principal Engineer & System Architect, Intel</i> <i>Pete Fiacco, CTO, GigaIO Networks</i> <i>Bithika Khargharia, Former Principal Architect, Extreme Networks</i> <i>Dave Meyer, Chief Scientist, Brocade</i> <i>Ying Zhang, Software Engineer, Facebook</i>
	16:35 – 18:35	HEAD BUBBA MEMORIAL COCKTAIL RECEPTION

WEDNESDAY, AUGUST 30

MORNING	Keynote 9:00 – 10:00	Information Transfer in the era of 5G <i>David Allan, Ericsson</i>
	Optics & Networks for Science 10:30 – 12:00	<ul style="list-style-type: none"> A High Speed Hardware Scheduler for 1000-port Optical Packet Switches to Enable Scalable Data Centers Subchannel Scheduling for Shared Optical On-chip Buses Utilizing HPC Network Technologies in High Energy Physics Experiments
AFTERNOON	Topologies, Routing & Process Placement 13:30 – 15:00	<ul style="list-style-type: none"> On the Impact of Routing Algorithms in the Effectiveness of Queuing Schemes in High-Performance Interconnection Networks Placement of Virtual Network Functions in Hybrid Data Center Networks MPI Process and Network Device Affinitization for Optimal HPC Application Performance
	Invited Talk 15:15 – 16:00	Communication at the Speed of Memory <i>Paolo Faraboschi, HP</i>
	Efficient Network Design & Network Architecture 16:00-17:30	<ul style="list-style-type: none"> Characterizing Deep Learning over Big Data (DLoBD) Stacks on RDMA-capable Networks Low-Level Host Software Stack Optimizations to Improve Aggregate Fabric Throughput Userspace RDMA Verbs on Commodity Hardware using DPDK
	17:30 – 17:45	AWARDS & CLOSING REMARKS

